National Semiconductor

Desktop FDDI Handbook

DESKTOP FDDI
HANDBOOK

1992 Edition

DP83266 MACSI

DP83256/DP83257 PLAYER+

DP83220 CDL

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DP83266 MACSI Device (FDDI Media Access Controller and System Interface)

National Semiconductor

PRELIMINARY
October 1992

DP83266 MACSI™ Device (FDDI Media Access Controller and System Interface)

General Description

The DP83266 Media Access Controller and System Interface (MACSI) implements the ANSI X3T9.5 Standard Media Access Control (MAC) protocol for operation in an FDDI token ring and provides a comprehensive System Interface.

The MACSI device transmits, receives, repeats, and strips tokens and frames. It produces and consumes optimized data structures for efficient data transfer. Full duplex architecture with through parity allows diagnostic transmission and self testing for error isolation and point-to-point connections.

The MACSI device includes the functionality of both the DP83261 BMAC™ device and the DP83265 BSI-2™ device with additional enhancements for higher performance and reliability.

Features

- Over 9 kBytes of on-chip FIFO
- 5 DMA channels (2 Output and 3 Input)
- 12.5 MHz to 33 MHz operation
- Full duplex operation with through parity
- Supports JTAG boundary scan
- Real-time Void stripping indicator for bridges
- On-chip address bit swapping capability
- 32-bit wide Address/Data path with byte parity
- Programmable transfer burst sizes of 4 or 8 32-bit words
- Receive frame filtering services
- Frame-per-Page mode controllable on each DMA channel
- Demultiplexed Addresses supported on ABus
- New multicast address matching feature
- ANSI X3T9.5 MAC standard defined ring service options
- Supports all FDDI Ring Scheduling Classes (Synchronous, Asynchronous, etc.)
- Supports Individual, Group, Short, Long and External Addressing
- Generates Beacon, Claim, and Void frames
- Extensive ring and station statistics gathering
- Extensions for MAC level bridging
- Enhanced SBus compatibility
- Interfaces to DRAMs or directly to system bus
- Supports frame Header/Info splitting
- Programmable Big or Little Endian alignment

Block Diagram

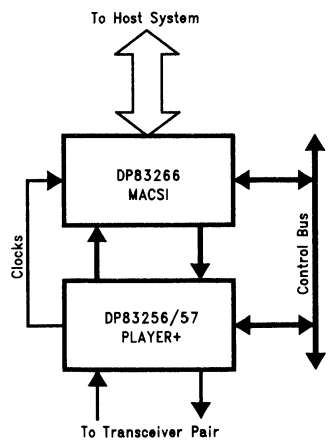

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FIGURE 1-1. FDDI Chip Set Block Diagram

RRD-B20M102/Printed in U. S. A.

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1.0 FDDI Chip Set Overview

National Semiconductor's FDDI chip set is shown in *Figure 1-1.* For more information about the PLAYER+™ device, consult the appropriate datasheet and application notes.

DP83256/57 PLAYER+ Device Physical Layer Controller

The PLAYER+ device implements the Physical Layer (PHY) protocol as defined by the ANSI FDDI PHY X3T9.5 Standard along with all the necessary clock recovery and clock generation functions.

Features

- Single chip FDDI Physical Layer (PHY) solution
- Integrated Digital Clock Recovery Module provides enhanced tracking and greater lock acquisition range
- Integrated Clock Generation Module provides all necessary clock signals for an FDDI system from an external 12.5 MHz reference
- Alternate PMD Interface (DP83257) Supports UTP twisted pair FDDI PMDS with no external clock recovery or clock generations functions required
- No External Filter Components
- Connection Management (CMT) Support (LEM, TNE, PC_React, CF_React, Auto Scrubbing)
- Full on-chip configuration switch
- Low Power CMOS-BIPOLAR design using a single 5V supply
- Full duplex operation with through parity
- Separate management interface (Control Bus)
- Selectable Parity on PHY-MAC Interface and Control Bus Interface
- Two levels of on-chip loopback
- 4B/5B encoder/decoder
- Framing logic
- Elasticity Buffer, Repeat Filter, and Smoother
- Line state detector/generator
- Supports single attach stations, dual attach stations and concentrators with no external logic
- DP83256 for SAS/DAS single path stations
- DP83257 for SAS/DAS single/dual path stations

In addition, the DP83256/57 contains an additional PHY_Data.request and PHY_Data.indicate port required for concentrators and dual attach stations.

DP83266 MACSI Device Media Access Controller and System Interface

The MACSI device implements the Timed Token Media Access Control protocol defined by the ANSI FDDI X3T9.5 MAC Standard as well as a high performance system interface.

Features

- Over 9 kBytes of on-chip FIFO
- 5 DMA channels (2 Output and 3 Input)
- 12.5 MHz to 33 MHz operation
- Full duplex operation with through parity
- Supports JTAG boundary scan
- Real-time Void stripping indicator for bridges
- On-chip address bit swapping capability
- 32-bit wide Address/Data path with byte parity
- Programmable transfer burst sizes of 4 or 8 32-bit words
- Receive frame filtering services
- Frame-per-Page mode controllable on each DMA channel
- Demultiplexed Addresses supported on ABus
- New multicast address matching feature
- ANSI X3T9.5 MAC standard defined ring service options
- Supports all FDDI Ring Scheduling Classes (Synchronous, Asynchronous, etc.)
- Supports Individual, Group, Short, Long and External Addressing
- Generates Beacon, Claim, and Void frames
- Extensive ring and station statistics gathering
- Extensions for MAC level bridging
- Enhanced SBus compatibility
- Interfaces to DRAMs or directly to system bus
- Supports frame Header/Info splitting
- Programmable Big or Little Endian alignment

2.0 General Features

The DP83266 MACSI device is a highly integrated FDDI controller. Together with the DP83256/57 PLAYER+ device, it forms a full-featured, high performance FDDI chip set useful for designing end station attachments, concentrators, bridges, routers, and other FDDI connections. The MACSI device provides all of the features and services of both the DP83261 BMAC device and the DP83265 BSI-2 device with enhanced performance and reliability.

For system connection, the MACSI device provides a simple yet powerful bus interface and memory management scheme to maximize system efficiency and it is capable of interfacing to a variety of host buses/environments. The MACSI device provides a 32-bit wide data interface, which can be configured to share a system bus to main memory or to use external shared memory. Also provided are 28-bit addresses multiplexed on the data pins as well as demultiplexed on dedicated pins. The system interface supports virtual addressing using fixed-size pages.

For network connection, the MACSI device provides many services which simplify network management and increase system performance and reliability. The MACSI device is capable of batching confirmation and indication status, filtering MAC frames with the same Information field as well as Void frames, and performing network monitoring functions.

2.1 FDDI MAC SUPPORT

The MACSI device implements the ANSI X3T9.5 FDDI MAC standard protocol for transmitting, receiving, repeating and stripping frames. The MACSI device provides all of the information necessary to implement the service primitives defined in the standard.

2.2 MAC ADDRESSING SUPPORT

Both long (48-bit) and short (16-bit) addressing are supported simultaneously, for both Individual and Group addresses.

2.3 MAC BRIDGING SUPPORT

Several features are provided to increase performance in bridging applications.

On the receive side, external address matching logic can be used to examine the PH_Indicate byte stream to decide whether to copy a frame, how to set the control indicators and how to increment the counters.

On the transmit side, transparency options are provided on the Source Address, the most significant bit of the Source Address, and the Frame Check Sequence (FCS).

In addition, support for an alternate stripping mechanism (implemented using My_Void frames) provides maximum flexibility in the generation of frames by allowing the use of Source Address Transparency (SAT).

2.4 MAC SERVICE CLASS SUPPORT

All FDDI MAC service classes are supported by the MACSI device including Synchronous, Asynchronous, Restricted Asynchronous, and Immediate service classes.

For Synchronous transmission, one or more frames are transmitted in accordance with the station's synchronous bandwidth allocation.

For Asynchronous transmission, one programmable asynchronous priority threshold is supported in addition to the threshold at the Negotiated Target Token Rotation time.

For Restricted Asynchronous transmission, support is provided to begin, continue and end restricted dialogues.

For Immediate transmissions, support is provided to send frames from either the Data, Beacon or Claim states and either ignore or respond to the received byte stream. After an immediate transmission a token may optionally be issued.

2.5 DIAGNOSTIC COUNTERS

The MACSI device includes a number of diagnostic counters and timers that monitor ring and station performance.

These counters allow measurement of the following:

- Number of frames transmitted and received by the station
- Number of frames copied as well as frames not copied
- Frame error rate of an incoming physical connection to the MAC
- Load on the ring based on the number of tokens received and the ring latency
- Ring latency
- Lost frames

The size of these counters has been selected to keep the frequency of overflow small, even under worst case operating conditions.

2.6 MANAGEMENT SERVICES

The MACSI device provides management services to the Host System via the Control Bus Interface. This interface allows access to internal registers to control and configure the MACSI device.

2.7 RING PARAMETER TUNING

The MACSI device includes settable parameters to allow tuning of the network to increase performance over a large range of network sizes.

The MACSI device supports systems of two stations with little cable between them to ring configurations much larger than the 1000 physical attachments and/or 200 kilometer distance that are specified as the default values in the standard.

The MACSI device also handles frames larger than the 4500 byte default maximum frame size as specified in the standard.

2.8 MULTI-FRAME STREAMING INTERFACE

The MACSI device provides an interface to support multi-frame streaming. Multiple frames can be transmitted after a token is captured within the limits of the token timer thresholds.

2.9 BEACON, CLAIM, AND VOID FRAMES GENERATION

For purposes of transient token and ring recovery, no processor intervention is required. The MACSI device automatically generates the appropriate MAC frames.

2.10 SELF TESTING

Since the MACSI device has a full duplex architecture, loopback testing is possible before entering the ring and during normal ring operation.

There are several possible loopback paths:

- Internal to the MACSI device
- Through the PLAYER+ device(s) using the PLAYER+ configuration switch
- Through the PLAYER+ Clock Recovery Module.

2.0 General Features (Continued)

These paths allow error isolation at the device level.

The MACSI device also supports through parity. Even when parity is not used by the system, parity support can be provided across the PHY Interface.

2.11 32-BIT ADDRESS/DATA PATH TO HOST MEMORY

The MACSI device provides a 32-bit wide synchronous data interface, which permits connection to a standard multimaster system bus operating from 12.5 MHz to 33 MHz, or to local memory, using Big or Little Endian byte ordering. Demultiplexed addresses are provided on dedicated pins. Address information is also multiplexed on the data pins to provide backward compatibility for designs based on the BSI device. The local memory may be static or dynamic. For maximum performance, the MACSI device uses burst mode transfers, with four or eight 32-bit words to a burst. To assist the user with the burst transfer capability, the three bits of the address which cycle during a burst are output as demultiplexed signals. Maximum burst speed is one 32-bit word per clock, but slower speeds may be accommodated by inserting wait states.

The MACSI device can operate within any combination of cached, non-cached, paged or non-paged memory environments. To provide this capability, all data structures are contained within a page boundary, and bus transactions never cross page boundaries. The MACSI device performs all bus transactions within aligned blocks to ease the interface to a cached environment.

2.12 MULTI-CHANNEL ARCHITECTURE

The MACSI device provides three Input Channels and two Output Channels, which are designed to operate independently and concurrently. They are separately configured by the user to manage the reception or transmission of a particular kind of frame (for example, synchronous frames only).

2.13 SUPPORT FOR HEADER/INFO SPLITTING

In order to support high performance protocol processing, the MACSI device can be programmed to split the header and information portions of (non-MAC/SMT) frames between two Indicate Channels. Frame bytes from the Frame Control field (FC) up to the user-defined header length are copied onto Indicate Channel 1, and the remaining bytes (Info) are copied onto Indicate Channel 2. This is useful for separating protocol headers from data and allows them to be stored in different regions of memory to prevent unnecessary copying. In addition, a protocol monitor application may decide to copy only the header portion of each frame.

2.14 MAC BRIDGING SUPPORT

Support for bridging and monitoring applications is provided by the Internal/External Sorting Mode. All frames matching the external address (frames requiring bridging) are sorted onto Indicate Channel 2, MAC and SMT frames matching the internal (Ring Engine) address are sorted onto Indicate Channel 0, and all other frames matching the device's internal address (short or long) are sorted onto Indicate Channel 1.

2.15 ADDRESS BIT SWAPPING

The MACSI contains the necessary logic for swapping the address fields within each frame between FDDI and IEEE Canonical bit order. This involves a bit reversal within each byte of the address field (e.g., 08-00-17-C2-A1-03 would become 10:00:E8:43:85:C0). This option is selectable on a per channel basis and is supported on all transmit and receive channels. This is useful for bridging FDDI to Ethernet or for swapping addresses for higher level protocols.

2.16 STATUS BATCHING SERVICES

The MACSI device provides status for transmitted and received frames. Interrupts to the host are generated only at status breakpoints, which are defined by the user on a per DMA Channel basis. Breakpoints are selected when the Channel is configured for operation. To allow batching, the MACSI provides a status option called Tend, that causes the device to generate a single Confirmation Message Descriptor (CNF) for one or more Request Descriptors (REQs).

The MACSI device further reduces host processing time by separating received frame status from the received data. This allows the CPU to scan quickly for errors when deciding whether further processing should be done on received frames. If status was embedded in the data stream, all data would need to be read contiguously to find the Status Indicator.

2.17 RECEIVE FRAME FILTERING SERVICES

To increase performance and reliability, the MACSI device can be programmed to filter out identical MAC (same FC and Info field) or SMT frames received from the ring. Void frames are filtered out automatically. Filtering unnecessary frames reduces the fill rate of the Indicate FIFO, reduces CPU frame processing time, and reduces memory bus transactions.

2.18 TWO TIMING DOMAINS

To provide maximum performance and system flexibility, the MACSI device uses two independent clocks, one for the MAC (ring) Interface, and one for the system/memory bus. The MACSI device provides a fully synchronized interface between these two timing domains.

2.19 CLUSTERED INTERRUPTS

The MACSI device can be operated in a polled or interrupt-driven environment. The MACSI device provides the ability to generate attentions (interrupts) at group boundaries. Some boundaries are pre-defined in hardware; others are defined by the user when the Channel is configured. This interrupt scheme significantly reduces the number of interrupts to the host, thus reducing host processing overhead.

2.20 FIFO MEMORY

The MACSI device contains over 9 kBytes of on-chip FIFO memory. This memory includes separate 4.6 kByte FIFOs for both the Transmit (Request) and Receive (Indicate) data paths. These data FIFOs allow the MACSI device to support over 370 μs of bus latency for both transmit and receive. They also allow the MACSI device to buffer entire maximum length FDDI frames on-chip for both transmit and receive simultaneously. This allows lower cost systems by enabling the MACSI device to reside directly on system buses with high latency requirements.

These FIFOs support all of the features available in the original BSI device including two transmit and three receive channels to make efficient use of the FIFO resources. New transmit thresholds are available to allow full use of the larger transmit FIFO.

2.0 General Features (Continued)

In addition to the 4.6 kByte data FIFOs, both the transmit and receive data paths contain Burst FIFO Blocks, each of which are organized as two banks of eight 32-bit words.

2.21 FRAME-PER-PAGE-PER-CHANNEL

The MACSI device has a feature which allows control of the Frame-per-Page mode (available on the BSI device) on a per-Channel basis. For example, this is useful in systems where Frame-per-Page mode is used to speed up memory space reclamation on an LLC channel, but where packing multiple frames into each page is desired to save space on the SMT channel.

2.22 COPY ALL MULTICAST

The MACSI provides a copy mode which allows all frames which are addressed with multicast addresses to be copied. Multicast addresses are those that have the Individual/Group address bit (most significant bit of the FDDI address) set. This simple scheme allows flexibility in the use of multicast addresses. The MACSI device copies all multicast frames and software makes the final determination as to which multicast groups this station belongs.

2.23 BRIDGE STRIPPING INFORMATION

The MACSI device provides an output designed to make it easier to build transparent bridges. Source Address Transparency features are provided as well as features to allow these frames to be stripped from the ring. For transparent bridges, it is important to know when the MACSI is using this stripping feature to remove frames from the ring which were forwarded by this bridge but with an unknown source address, (i.e., Source Address Transparency enabled). This is important because the bridge does not want to "learn" these addresses. This feature is provided by the MACSI in the form of an output pin indicating which frames contain addresses which should be added to the address filter table (i.e. learned).

2.24 JTAG BOUNDARY SCAN

The MACSI device supports the JTAG boundary scan standard (IEEE Std. 1149.1–1990).

3.0 Architectural Description

The MACSI is derived from the BMAC and BSI devices. The MACSI is composed of the Ring Engine, the Service Engine, and the Bus Interface Unit. The Ring Engine performs the FDDI MAC Timed token protocol and contains the MAC transmitter and receiver. The Service Engine implements the Request and Indicate Data Services and contains the Transmit and Receive Data FIFOs. The Bus Interface Unit implements the high speed synchronous bus handshake and contains the Burst FIFOs.

The MACSI device uses a full duplex architecture and provides sufficient bandwidth at the ABus for full duplex transmission with support for through parity. *Figure 3-1* shows the MACSI device architecture.

3.1 INTERFACES

3.1.1 PHY Interface

The PHY Interface is a synchronous interface that provides a byte stream to the PLAYER+ device (the PHY Request byte stream, PHY__Request), and receives a byte stream from the PLAYER+ device (the PHY Indicate byte stream, PHY__Indicate).

The 10 bits transferred in both directions across the PH__Indicate and PH__Request Interfaces consists of one parity bit (odd parity), one control bit, and 8 bits of data. The control bit determines if the 8 data bits are a data symbol pair or a control symbol pair.

3.1.2 ABus Interface

The ABus interface provides the high performance synchronous Data and Control interface to the Host System and/or local memory. Data and Descriptors are transferred via this interface over the 32-bit Data bus (with byte parity). Both multiplexed and non-multiplexed address information is available on this bus. Arbitration and transfer control signals are provided and minimize the requirements for external glue logic.

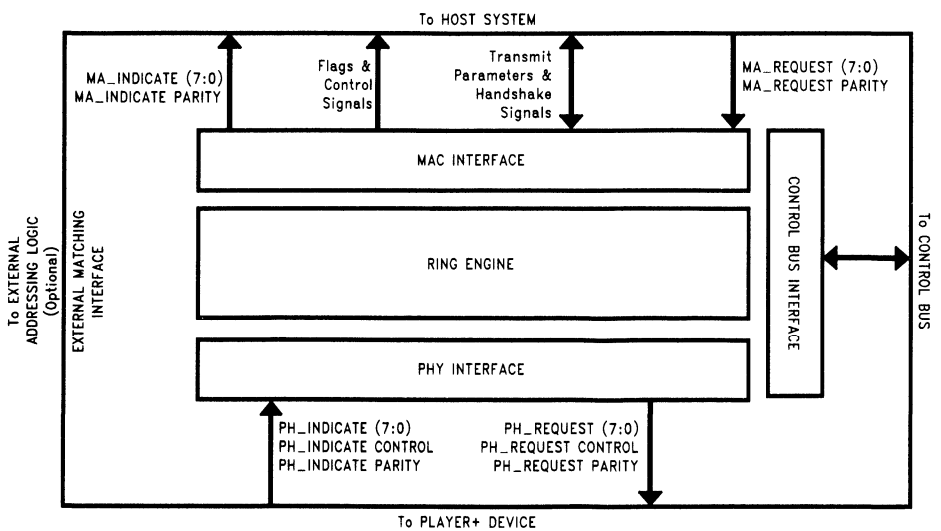

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FIGURE 3-1. MACSI Device Block Diagram

3.0 Architectural Description (Continued)

3.1.3 Control Bus Interface

The Control Interface implements the interface to the Control Bus which allows the user to initialize, monitor and diagnose the operation of the MACSI. The Control Interface is an 8-bit interface. This reduces the pinout and minimizes board space. All information that must be synchronized with the data stream crosses the ABus Interface.

The Control Bus is separated completely from the high performance data path in order to allow independent operation of the processor on the Control Bus. The Control Interface provides synchronization between the asynchronous Control Bus and the synchronous operation of the device.

During operation, the host uses the Control Bus to access the device's internal registers, and to manage the attention/notify (interrupt) logic.

3.2 RING ENGINE

The Ring Engine consists of four blocks: Receiver, Transmitter, MAC Parameter RAM, and Counters/Timers as shown in *Figure 3-2.*

3.2.1 Receiver

The Receiver accepts data from the PHY level device in byte stream format (PH_Indicate).

Upon receiving the data, the Receiver performs the following functions:

- Determines the beginning and ending of a Protocol Data Unit (PDU)
- Decodes the Frame Control field to determine the PDU type (frame or token)
- Compares the received Destination and Source Addresses with the internal addresses
- Processes data within the frame
- Calculates and checks the Frame Check Sequence at the end of the frame
- Checks the Frame Status field

And finally, the Receiver presents the data to the MAC Interface along with the appropriate control signals (MA_Indicate).

3.2.2 Transmitter

The Transmitter inserts frames from this station into the ring in accordance with the FDDI Timed-Token MAC protocol. It also repeats frames from other stations in the ring. The Transmitter block multiplexes data from the MA_Request Interface and data from the Receiver Block. During frame transmission, data from the Request Interface is selected. During frame repeating, data from the Receiver is selected.

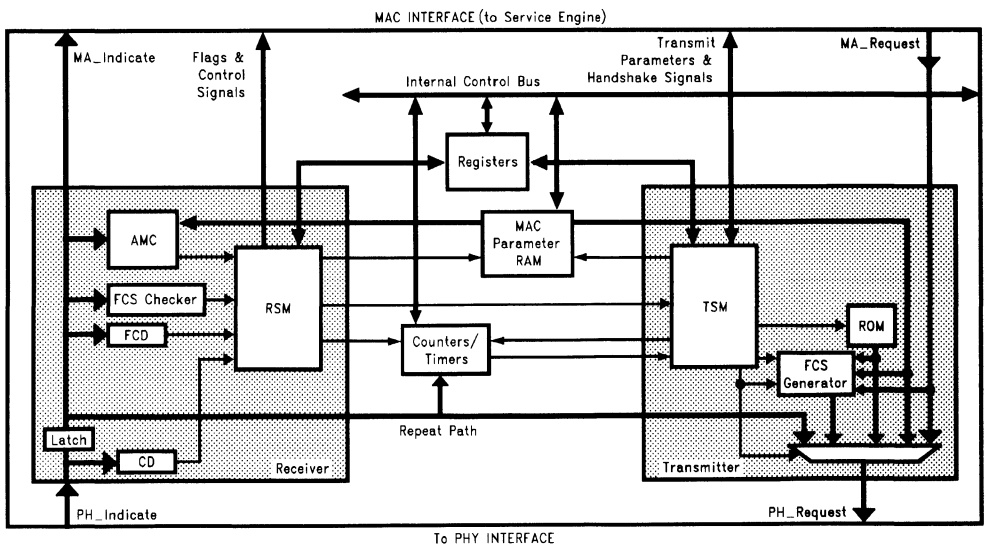

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FIGURE 3-2. Ring Engine Block Diagram

3.0 Architectural Description (Continued)

During frame transmission, the Transmitter performs the following functions:

- Captures a token to gain the right to transmit
- Transmits one or more frames
- Generates the Frame Check Sequence and appends it at the end of the frame
- Generates the Frame Status field that is transmitted at the end of the frame
- Issues the token at the end of frame transmission

During frame repeating, the Transmitter performs the following functions:

- Repeats the received frame and modifies the Frame Status field at the end of the frame as specified by the standard

Whether transmitting or repeating frames, the Transmitter also performs the following functions:

- Strips the frame(s) that are transmitted by this station
- Generates Idle symbols between frames

Data is presented from the Transmitter to the PLAYER+ device in byte stream format (PH_Request).

3.2.3 MAC Parameter RAM

The MAC Parameter RAM is a dual port RAM that contains MAC parameters such as the station's short and long addresses. These parameters are initialized via the Control Interface. Both the Receiver and Transmitter Blocks access the RAM.

The Receiver uses these parameters to compare addresses in incoming frames with the individual and group addresses stored in the Parameter RAM.

The Transmitter uses the Parameter RAM for generating the Source Address for all frames (except when Source Address Transparency is enabled) and for the Destination Address and Information fields on Claim and Beacon frames.

3.2.4 Counters/Timers

The Counter/Timer Block maintains all of the counters and timers required by the ANSI X3T9.5 MAC standard.

Events which occur too rapidly for software to count, such as the various Frame Counts, are included in the Event Counters. The size of the wrap around counters has been chosen to require minimal software intervention even under marginal operating conditions. Most of the counters increment in response to events detected by the Receiver. The counters are readable via the Control Interface.

The Token Rotation and Token Holding Timers which are used to implement the Timed Token Protocol are contained within the Timer Block.

3.3 DATA STRUCTURES

3.3.1 Data Types

The architecture of the MACSI device defines two basic types of objects: Data Units and Descriptors. A Data Unit is a group of contiguous bytes which forms all or part of a frame. A Descriptor is a two-word (64-bit) control object that provides addressing information and control/status information about MACSI device operations.

Data and Descriptor objects may consist of one or more parts, where each part is contiguous and wholly contained within a memory page. Descriptor pages are selectable as all 1 kBytes or all 4 kBytes. Data Units are described by Descriptors with a pointer and a count. A single Data Unit may not cross a 4k boundary. All Descriptors may be marked as **First, Middle, Last,** or **Only.** Thus, multiple Descriptors may be combined to describe a single entity (i.e. one frame). A single-part object consists of one **Only** Part; a multiple-part object consists of one **First** Part, zero or more **Middle** Parts, and one **Last** Part. In Descriptor names, the object part is denoted in a suffix, preceded by a dot. Thus an Input Data Unit Descriptor (IDUD), which describes the last Data Unit of a frame received from the ring, is called an IDUD.Last.

A Data Unit is stored in contiguous locations within a single 4 kByte page in memory. Multiple-part Data Units are stored in separate, and not necessarily contiguous 4 kByte pages. Descriptors are stored in contiguous locations in Queues and Lists, where each Queue occupies a single 1 kByte or 4 kByte memory page, aligned on the queue-size boundary. For Queues, an access to the next location after the end of a page will automatically wrap-around and access the first location in the page.

Data Units are transferred between the MACSI's Service Engine and Ring Engine via five simplex Channels, three used for Indicate (receive) data and two for Request (transmit) data. Parts of frames received from the ring and copied to memory are called Input Data Units (IDUs); parts of frames read from memory to be transmitted to the ring are called Output Data Units (ODUs).

Descriptors are transferred between the MACSI device and Host via the ABus, whose operation is for the most part transparent to the user. There are five Descriptor types recognized by the MACSI device: Input Data Unit Descriptors (IDUDs), Output Data Unit Descriptors (ODUDs), Pool Space Descriptors (PSPs), Request Descriptors (REQs), and Confirmation Message Descriptors (CNFs).

Input and Output Data Unit Descriptors describe a single Data Unit part, i.e., its address (page number and offset), its size in bytes, and its part (Only, First, Middle, or Last). Frames consisting of a single part are described by a Descriptor.Only; frames consisting of multiple parts are described by a single Descriptor.First, zero or more Descriptor.Middles, and a single Descriptor.Last.

Every Output Data Unit part is described by an ODUD. Output Data Unit Descriptors are fetched from memory so that frame parts can be assembled for transmission.

Every Input Data Unit part is described by an Input Data Unit Descriptor (IDUD). Input Data Unit Descriptors are generated on Indicate Channels to describe where the MACSI device wrote each frame part and to report status for the frame.

Request Descriptors (REQs) are written by the user to specify the operational parameters for the MACSI device Request operations. Request Descriptors also contain the start address of part of a stream of ODUDs and the number of frames represented by the ODUD stream part (i.e., the number of ODUD.Last descriptors). Typically, the user will define a single Request Object consisting of multiple frames of the same request and service class, frame control, and expected status.

3.0 Architectural Description (Continued)

Confirmation Messages (CNFs) are created by the MACSI device to record the result of a Request operation.

Pool Space Descriptors (PSPs) describe the location and size of a region of memory space available for writing Input Data Units.

Request (transmit) and Indicate (receive) data structures are summarized in *Figure 3-3.*

3.3.2 Descriptor Queues and Lists

The MACSI device uses 10 Queues and two Lists which are circular. There are six Queues for Indicate operations, and four Queues and two Lists for Request operations. Each of the three Indicate Channels has a Data Queue containing Pool Space Descriptors (PSPs), and a Status Queue containing Input Data Unit Descriptors (IDUDs). Each Request Channel has a Data Queue containing Request Descriptors (REQs), a Status Queue containing Confirmation Messages (CNFs), and a List containing Output Data Unit Descriptors (ODUDs).

During Indicate and Request operations, Descriptor Queues and Lists are read and written by the MACSI device, using registers in the Pointer and Limit RAM Register files. The Pointer RAM Queue and List Pointer Registers point to a location from which a Descriptor will be read (PSPs and REQs) or written (IDUDs and CNFs). All of the Queues and Lists are strictly unidirectional. The MACSI consumes objects in those queues which are produced by the Host. The Host consumes objects in those queues which are produced by the MACSI.

For each Queue Pointer Register there is a corresponding Queue Limit Register in the Limit RAM Register file, which holds the Queue's limit as an offset value in units of 1 Descriptor (8 bytes). The address in the Queue Pointer is incremented before a Descriptor is read and after a Descriptor is written, then compared with the value in the corresponding Queue Limit Register. When a Queue Pointer Register becomes equal to the Queue Limit Register, an attention is generated, informing the host that the Queue is empty. When a pointer value is incremented past the end of the page, it wraps to the beginning of the page.

3.3.3 Storage Allocation

The maximum unit of contiguous storage allocation in external memory is a Page. All MACSI device addresses consist of a 16-bit page number and a 12-bit offset.

The MACSI device uses a page size of 1 kByte or 4 kBytes for storage of Descriptor Queues and Lists (as selected by the user), and a page size of 4 kBytes for storage of Data Units. A single page may contain multiple Data Units, and multiple-part Data Units may span multiple, disjoint or contiguous pages.

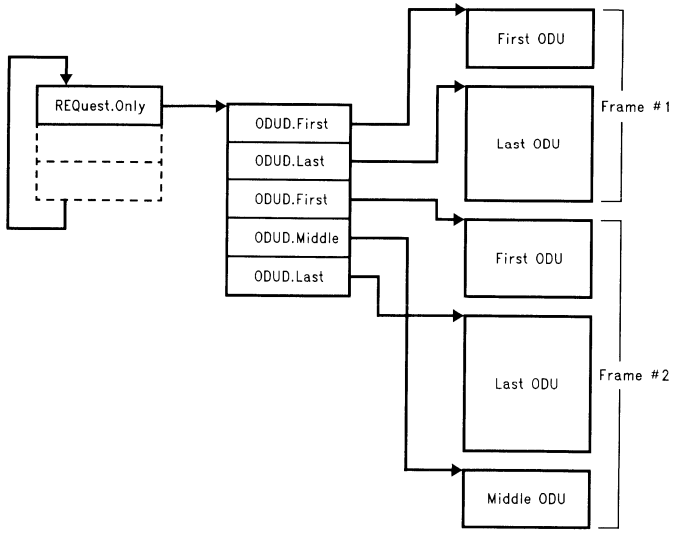
3.4 SERVICE ENGINE

The Service Engine, which manages the operation of the MACSI, contains seven basic blocks: Indicate Machine, Request Machine, Status/Space State Machine, Pointer RAM, Limit RAM, and Bus Interface Unit. An internal block diagram of the Service Engine is shown in *Figure 3-4.*

3.4.1 Indicate Machine

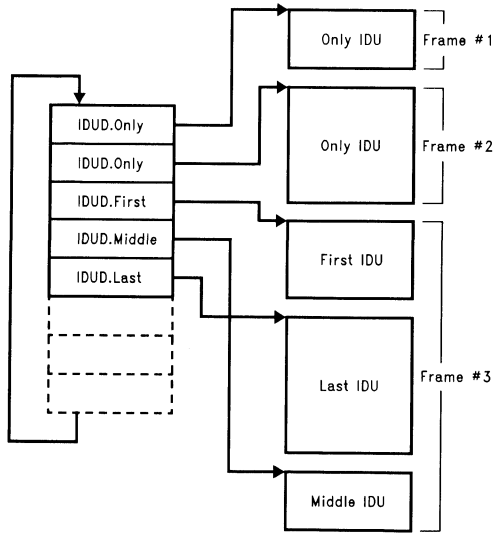
The Indicate Block accepts Service Data Units (frames) from the Ring Engine (MAC) in a byte stream format (MA_Indicate).

Request Data Structures



TL/F/11705–4

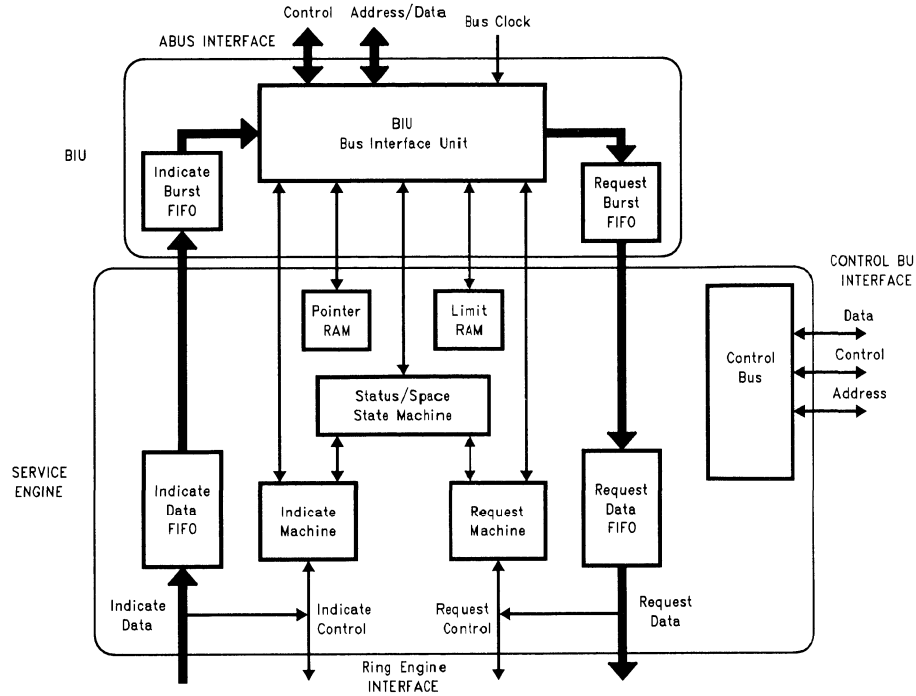
Indicate Data Structures



TL/F/11705–5

FIGURE 3-3. MACSI Device Data Structures

3.0 Architectural Description (Continued)



TL/F/11705–6

FIGURE 3-4. Service Engine/BIU Internal Block Diagram

Upon receiving the data, the Indicate Block performs the following functions:

- Decodes the Frame Control field to determine frame type
- Sorts received frames onto Channels according to the Sort Mode
- Optionally Filters identical MAC frames
- Filters Void frames
- Copies the received frames to memory according to Copy Criteria
- Writes status for the received frames to the Indicate Status Queue
- Issues interrupts to the host at host-defined status breakpoints

3.4.2 Request Machine

The Request Machine presents frames to the Ring Engine (MAC) in a byte stream format (MA_Request).

The Request Machine performs the following functions:

- Reads frames from host memory and assembles them onto Request Channels
- Prioritizes active requests
- Transmits frames to the Ring Engine (MAC)
- Optionally writes status for transmitted and returning frames
- Issues interrupts to the host on user-defined group boundaries

3.4.3 Status/Space Machine

The Status/Space Machine is used by both the Indicate Machine and the Request Machine.

The Status/Space Machine manages all descriptor Queues and writes status for received and transmitted frames.

3.4.4 Bus Interface Unit

The Bus Interface Unit (BIU) is used by both the Indicate and Request Blocks. It manages the ABus Interface, providing the MACSI device with a 32-bit data path to local or system memory.

The Bus Interface Unit controls the transfer of Data Units and Descriptors between the MACSI device and Host memory via the ABus.

Data and Descriptors are transferred between the MACSI device and Host memory. Each Channel type handles a set of Data and Descriptor objects. The three Indicate (Receive) Channels use the following objects:

1. Input Data Units (written by MACSI)
2. Input Data Unit Descriptors (written by MACSI)
3. Pool Space Descriptors (read by MACSI)

The two Request (Transmit) Channels each use the following objects:

1. Output Data Units (read by MACSI)
2. Output Data Unit Descriptors (read by MACSI)
3. Confirmation Message Descriptors (written by MACSI)
4. Request Descriptors (read by MACSI)

3.0 Architectural Description
(Continued)

Each Channel will only process one object type at a time. The BIU arbitrates between the Channels and issues a Bus Request when any Channel requests service. The priority of Channel bus requests is as follows, from highest priority to lowest priority:

1. Indicate Data Unit writes (highest priority when not transmitting)
2. Output Data Unit fetches (highest priority when transmitting)
3. Request Descriptor and Output Data Unit Descriptor fetches
4. Input Data Unit Descriptor writes
5. Confirmation Message Descriptor writes
6. Next Pool Space Descriptor transfer to Current Pool Space Descriptor (internal operation)
7. Pool Space Descriptor fetches
8. Limit RAM Operations (internal operation)
9. Pointer RAM Operations (lowest priority)

Addresses for Channel accesses are contained in the Pointer RAM Registers.

3.4.5 Pointer RAM

The Pointer RAM Block is used by both the Indicate and Request Machines. It contains pointers to all Data Units and Descriptors manipulated by the MACSI device, namely, Input and Output Data Units, Input and Output Data Unit Descriptors, Request Descriptors, Confirmation Message Descriptors, and Pool Space Descriptors.

The Pointer RAM Block is accessed by clearing the PTOP (Pointer RAM Operation) bit in the Service Attention Register, which causes the transfer of data between the Pointer RAM Register and a mailbox location in memory.

3.4.6 Limit RAM

The Limit RAM Block is used by both the Indicate and Request Machines. It contains data values that define the limits of the ten Queues maintained by the MACSI device.

Limit RAM Registers are accessed by clearing the LMOP (Limit RAM Operation) bit in the Service Attention Register, which causes the transfer of data between the Limit RAM Register and the Limit Data and Limit Address Registers.

4.0 FDDI MAC Facilities

4.1 SYMBOL SET

The Ring Engine (MAC) recognizes and generates a set of symbols. These symbols are used to convey Line States (such as the Idle Line State), Control Sequences (such as the Starting and Ending Delimiters) and Data.

Additional information regarding the symbol set can be found in the ANSI X3T9.5 PHY standard.

The Ring Engine expects that the Starting Delimiter will always be conveyed on an even symbol pair boundary (i.e., the JK symbol will always arrive as a byte, not split across two bytes). Following the starting delimiter, data symbols should always come in matched pairs. Similarly the Ending Delimiter should always come in one or more matched symbol pairs.

The symbol pairs conveyed at the PHY Interface are shown in Table 4-1.

4.2 PROTOCOL DATA UNITS

The Ring Engine recognizes and generates Tokens and Frames.

The Token is used to control access to the ring. Only the station that has captured the token has the right to transmit new information. The format of a token is shown in *Figure 4-1.*

TABLE 4-1. Symbol Pair Set

Type	Symbols
Starting Delimiter	JK or IL
Ending Delimiter	TT or TR or TS or TI
Frame Status	RR or RS or SR or SS
Idle	II or nI
Data Pair	nn

n represents any data symbol (0–F).

Symbol pairs other than the defined symbols are treated as code violations.

Additional information on the symbol pairs generated and interpreted by the Ring Engine can be found in Section 8.2.1.

TABLE 4-2. Frame Fields

Name	Description	Size
SFS	Start of Frame Sequence	
PA	Preamble	8 or more Idle symbol pairs
SD	Starting Delimiter	JK symbol pair
FC	Frame Control Field	1 data symbol pair
DA	Destination Address	2 or 6 symbol pairs
SA	Source Address	2 or 6 symbol pairs
INFO	Information Field	
FCS	Frame Check Sequence	4 symbol pairs
EFS	End of Frame Sequence	
ED	Ending Delimiter	at least 1 T symbol for Frames; at least 2 T symbols for Tokens
FS	Frame Status	3 or more R or S symbols

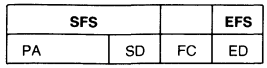


FIGURE 4-1. Token Format

Frames are used to pass information between stations. The format of a frame is shown in *Figure 4-2,* with the field definitions in Table 4-2.

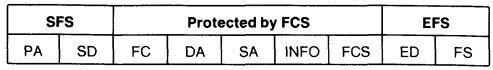


FIGURE 4-2. Frame Format

4.0 FDDI MAC Facilities (Continued)

4.2.1 Frame Fields

Start of Frame Sequence (SFS)

The Start of Frame Sequence consists of the Preamble (PA) followed by the Starting Delimiter (SD).

The Preamble is a sequence of zero or more Idle symbols that is used to separate frames. The Ring Engine Receiver can process and repeat a frame or token with no preamble. The Ring Engine Transmitter generates frames with at least 8 bytes of preamble. The Ring Engine Transmitter also guarantees that valid FDDI frames will never be transmitted with more than 40 bytes of preamble.

The Starting Delimiter is used to indicate the start of a new frame. The Starting Delimiter is the JK Symbol pair.

The Ring Engine expects the Starting Delimiter to be conveyed across the PH_Indication Interface as a single byte. Similarly, the Ring Engine only generates Starting Delimiters aligned to the byte boundary.

Frame Control (FC)

The Frame Control field is used to discriminate frames. For tokens, the FC field identifies Restricted and Non-restricted tokens. For other frames, the FC field identifies the frame type and format and how the frame is to be processed.

The one byte FC field is formatted as shown in *Figure 4-3*.

C	L	F	F	r	Z	Z	Z

FIGURE 4-3. Frame Control Field

The C (Class) bit specifies the MAC Service Class as Asynchronous (C = 0) or Synchronous (C = 1).

The L (Length) bit specifies the length of the MAC Address as Short (L = 0) or Long (L = 1). A Short Address is a 16-bit address. A Long Address is a 48-bit address.

The FF (Format) bits specify the frame types as shown in Table 4-3.

The r (Reserved) bit is currently not specified and should always be transmitted as Zero.

The ZZZ (Control) bits are used in conjunction with the C and FF bits to specify the type of frames. These bits may be used to affect protocol processing criteria such as the Priority, Protocol Class, Status Handling, etc.

TABLE 4-3. Frame Control Format Bits

FC.FF		Frame Types
0	0	SMT/MAC
0	1	LLC
1	0	reserved for implementer
1	1	reserved for future standardization

When the Frame Control Format bits (FC.FF) indicate an SMT or MAC frame, the frame type is identified as shown in Table 4-4.

TABLE 4-4. MAC/SMT Frame Types

CLFF	rZZZ	Frame Type
1000	0000	Non-restricted Token
1100	0000	Restricted Token
0L00	0000	Void Frame
0L00	0001 to 1110	SMT Frame
0L00	1111	SMT Next Station Addressing Frame
1L00	0001	Other MAC Frame
1L00	0010	MAC Beacon Frame
1L00	0011	MAC Claim Frame
1L00	0100	MAC Purge Frame
1L00	0101 to 1111	Other MAC Frame

Destination Address (DA)

The Destination Address (DA) field is used to specify the station(s) that should receive and process the frame.

The DA can be an Individual or Group address. This is determined by the Most Significant Bit of the DA (DA.IG). When DA.IG is 0 the DA is an Individual Address, when DA.IG is 1 the DA is a Group Address. The Broadcast/Universal address is a Group Address.

The DA field can be a Long or Short Address. This is determined by the L bit in the FC field (FC.L). If FC.L is 1, the DA is a 48-bit Long Address. If FC.L is 0, the DA is a 16-bit Short Address.

The Ring Engine maintains a 16-bit Individual Address (My Short Address (MSA)), and a 48-bit Individual Address (My Long Address (MLA)).

On the receive side, if DA.IG is 0 the incoming DA is compared with MLA (if FC.L = 1) or MSA (if FC.L = 0). If the received DA matches MLA or MSA the frame is intended for this station and the address recognized flag (A_Flag) is set. If DA.IG is 1, the DA is a Group Address and is compared with the set of Group Addresses recognized by the Ring Engine. If a match occurs the address recognized flag (A_Flag) is set. The A_Flag is used by system interface logic as part of the criteria (with FC.L, DA.IG and M_Flag) to determine whether or not to copy the frame. If the A_Flag is set, the system interface will normally attempt to copy the frame.

On the transmit side, the DA is provided by the system interface logic as part of the data stream. The length of the address to be transmitted is determined by the L bit of the FC field. (The FC field is also passed in the data stream.) The Destination Address can be an Individual, Group, or Broadcast Address.

Source Address (SA)

The Source Address (SA) field is used to specify the address of the station that originally transmitted the frame.

The Source Address has the same length as the Destination Address (i.e., if the DA is a 16-bit Address, the SA is a 16-bit Address; if the DA is a 48-bit Address, the SA is a 48-bit Address).

4.0 FDDI MAC Facilities (Continued)

On the receive side, the incoming SA is compared with either MSA or MLA. If a match occurs between the incoming SA and this station's MLA or MSA, the MFlag is set. This flag is used to indicate that the frame is recognized as having been transmitted by this station and is stripped. The most significant bit of the SA (SA.IG) is not evaluated in the comparison.

On the transmit side, the station's individual address is transmitted as the SA. Since the SA field is normally used for stripping frames from the ring, the SA stored by the Ring Engine normally replaces the SA from the data stream. The length of the address to be transmitted is determined by the L bit of the FC field. (The FC field is passed in the data stream.) The most significant bit of the SA (SA.IG) is normally transmitted as 0, independent of the value passed through the data stream.

As a transmission option, the SA may also be transmitted transparently from the data stream. When the SA Transparency option is used, an alternate stripping mechanism is necessary to remove these frames from the ring. (The Ring Engine provides a Void Stripping Option; see Request Channel 0 and 1 Configuration Registers 0 (R0CR0 and R1CR0) for further information.)

As a separate and independent transmission option, the MSB of the SA may also be transmitted transparently from the data stream. This is useful for end stations participating in the Source Routing protocol that would like to continue to perform reliable stripping based on the SA. (When this option is used without SAT, the transmitted SA is generated by the Ring Engine, as always.)

Information (INFO)

The Information field contains the data transferred between peer users of the MAC data service (SMT, LLC, etc.). There is no INFO field in a Token.

The INFO field contains zero or more bytes.

On the receive side, the INFO field is checked to ensure that it has at least the minimum length for the frame type and contains an even number of symbols, as required by the ANSI X3T9.5 MAC standard.

The first 4 bytes of the INFO field of MAC frames are stored in an internal register and compared against the INFO field of the next MAC frame. If the data of the two frames match and both frames were MAC frames, the SameInfo signal is generated. This signal may be used to copy MAC frames only when new information is present.

On the transmit side, the Ring Engine does not limit the maximum size of the INFO field, but it does insure that frames are transmitted with a valid DA and SA.

Frame Check Sequence (FCS)

The Frame Check Sequence is a 32-bit Cyclic Redundancy Check that is used to check for data corruption in frames. There is no FCS field in a Token.

On the receive side, the Ring Engine checks the FCS to determine whether the frame is valid or corrupted.

On the transmit side, the FCS field is appended to the end of the INFO field. As a transmission option, appending the FCS to the frame can be inhibited (FCS Transparency).

End of Frame Sequence (EFS)

The End of Frame Sequence (EFS) always begins with a T symbol and should always contain an even number of symbols. For Tokens, an additional T symbol is added. For frames, the Ending Delimiter (ED) is followed by one or more of Frame Status Indicators (FS).

The Frame Status (FS) field is used to indicate the status of the frame. The FS field consists of three Indicators: Error Detected (E), Address Recognized (A), and Frame Copied (C). These Indicators are created and modified as specified in the ANSI X3T9.5 MAC standard.

For frames transmitted by the Ring Engine, the E, A and C Indicators are appended to all frames and are transmitted as R symbols. No provisions are made to generate additional trailing control indicators.

For frames repeated by the Ring Engine, the E, A and C Indicators are handled as specified in the Standard. Additional trailing control indicators are repeated unmodified provided they are properly aligned. See Section 5.5 for details on Frame Status Processing.

4.2.2 Token Formats

The Ring Engine supports non-restricted and restricted Tokens. See *Figure 4-4* and *Figure 4-5*.

SFS	FC	EFS
SD	80	ED

FIGURE 4-4. Non-Restricted Token Format

SFS	FC	ED
SD	C0	ED

FIGURE 4-5. Restricted Token Format

Non-restricted

A non-restricted token is used for synchronous and non-restricted asynchronous transmissions. Each time the non-restricted token arrives, a station is permitted to transmit one or more frames in accordance with its synchronous bandwidth allocation regardless of the status of the token (late or early).

Asynchronous transmissions occur only if the token is early (usable token) and the Token Holding Timer has not reached the selected threshold.

Restricted

A restricted token is used for synchronous and restricted asynchronous transmissions only.

A station which initiates the restricted dialogue captures a non-restricted token and releases a restricted token. Stations that participate in the restricted dialogue are allowed to capture the restricted token. A station ends the restricted dialogue by capturing the restricted token and releasing a non-restricted token.

4.2.3 Frame Formats

The Ring Engine supports all of the frame formats permitted by the FDDI standard. All frame types may be created extemal to the Ring Engine and be passed through the MAC Request Interface to the Ring. The Ring Engine also has the ability to generate Void, Beacon, and Claim frames internally.

4.0 FDDI MAC Facilities (Continued)

Frames Generated Externally

The Ring Engine transmits frames passed to it from the System Interface. The data portion of the frame is created by the System Interface. The data portion begins with the FC field and ends with the last byte of the INFO field. The FC field is passed transparently to the ring. The length bit in the FC field is used to determine the length of the transmitted addresses. The data is passed as a byte stream across the MAC Request Interface as shown in Table 4-5.

TABLE 4-5. Frame Formats

Field	Size (bytes)	MA_Request	PH_Request
PA	≥8; ≤40		Idle Pairs
SD	1		JK
FC	1	FC	FC
DA	2 or 6	DA	DA
SA	2 or 6	SA	MSA, MLA, or SA
INFO	≥0	INFO	INFO
FCS	4 if present	FCS	FCS
ED	1		TR
FS	1		RR

Before the frame is transmitted, the Ring Engine inserts the Start of Frame Sequence with at least 8 bytes of Preamble but no more than 40 bytes of Preamble. The starting delimiter is transmitted as a JK symbol pair. The Source Address is normally transmitted by the Ring Engine since it uses the Source Address to determine when to strip a frame from the ring. This can be overridden by using the Source Address transparency capability. Similarly, the Frame Check Sequence (4 bytes) is normally transmitted by the Ring Engine. This can be overridden with the FCS transparency capability. With FCS transparency, the FCS is transmitted from the data stream. The End of Frame Sequence is always transmitted by the Ring Engine as TR RR.

Frames Generated by Ring Engine

The Ring Engine generates and detects several frames in order to attain and maintain an operational ring.

Void Frames

Void frames are used during normal operation. The Ring Engine generates two types of void frames: regular Void frames and My_Void frames.

If Short addressing is enabled, Void frames with the short address (MSA) are transmitted. Otherwise, Void frames with the long address (MLA) are transmitted. Table 4-6 shows the Void frame format.

Void frames are transmitted in order to reset the Valid Transmission timers (TVX) in other stations to eliminate unnecessary entry to the Claim state. Stations are not required to copy Void frames. Void frames are transmitted by the Ring Engine in two situations:

1. While holding a token when no data is ready to be transmitted.
2. After a frame transmission is aborted.

My_Void frames are transmitted by the Ring Engine in three situations:

1. After a request to measure the Ring Latency has been made and the next early token is captured.
2. After this station wins the Claim process and before the token is issued.
3. After a frame has been transmitted with the STRIP option and before the token for that service opportunity is issued.

Void frames are also detected by the Ring Engine. A Void frame with a Source Address other than MSA or MLA is considered an Other_Void frame.

Claim Frames

Claim frames are generated continuously with minimum preamble while the Ring Engine is in the Transmit Claim state.

The format of Claim frames generated by the Ring Engine is shown in Table 4-7. When long addressing is enabled, frames with the long address (MLA) are transmitted. Otherwise frames with the short address (MSA) are transmitted.

The Ring Engine detects reception of valid Claim frames. A comparison is performed between the first four bytes of the received INFO field and the value of TREQ programmed in the parameter RAM in order to distinguish Higher_Claim, Lower_Claim, Duplicate_Claim, and My_Claim.

Beacon Frames

Beacon frames are transmitted continuously with minimum preamble when the Ring Engine is in the Transmit Beacon state. The format of Beacon frames generated by the Ring Engine is shown in Table 4-8. When long addressing is enabled, frames with the long address (MLA) are transmitted. Otherwise frames with the short address (MSA) are transmitted.

TABLE 4-6. Void Frames

Type	Enable	Size	SFS		FC	DA	SA	FCS	EFS
Void	ESA	Short	PA	SD	40	null	MSA	FCS	TRRR
Void	not ESA	Long	PA	SD	00	null	MLA	FCS	TRRR
My__Void	ESA	Short	PA	SD	40	MSA	MSA	FCS	TRRR
My__Void	not ESA	Long	PA	SD	00	MLA	MLA	FCS	TRRR

TABLE 4-7. Claim Frames

Type	Enable	Size	SFS		FC	DA	SA	INFO	FCS	EFS
My__Claim	not ELA	Short	PA	SD	83	MSA	MSA	TREQ	FCS	TRRR
My__Claim	ELA	Long	PA	SD	C3	MLA	MLA	TREQ	FCS	TRRR

TABLE 4-8. Beacon Frames

Type	Enable	Size	SFS		FC	DA	SA	INFO	FCS	EFS
My__Beacon	not ELA	Short	PA	SD	82	null	MSA	TBT	FCS	TRRR
My__Beacon	ELA	Long	PA	SD	C2	null	MLA	TBT	FCS	TRRR

When the Transmit Beacon State is entered from the Transmit Claim State the first byte of the 4 byte TBT field is transmitted as Zero.

Beacon frames that require alternative formats such as Directed Beacons must be generated externally.

The Ring Engine detects reception of valid Beacon frames and distinguishes between Beacon frames transmitted by this MAC (My__Beacon) and Beacon frames transmitted by other stations (Other__Beacon).

4.3 FRAME COUNTS

To aid in fault isolation and to enhance the management capabilities of a ring, the Ring Engine maintains several frame counts. The Error and Isolated frame counts increment when a frame is received with one or more errors that were previously undetected. The Ring Engine then modifies the Error Control Indicator so that a downstream station will not increment its count.

The size of the counters has been chosen such that minimal software intervention is required, even under marginal operating conditions.

The following counts are maintained by the Ring Engine:

FRCT Frame Received

EICT Error Isolated

LFCT Lost Frame

FCCT Frames Copied with Ax set

FNCT Frames Not Copied with Ax set

FTCT Frames Transmitted

4.3.1 Frame Received Count (FRCT)

The Frame Received Count is described in the FDDI MAC standard, and is the count of all complete frames received. This count includes frames stripped by this station.

4.3.2 Error Isolated Count (EICT)

The Error Isolated Count is described in the FDDI MAC standard, and is the count of error frames detected by this station and no previous station. It increments when:

1. An FCS error is detected and the received Error Indicator (Er) is not equal to S.
2. A frame of invalid length (i.e., off boundary T) is received and Er is not equal to S.
3. Er is not R or S.

4.3.3 Lost Frame Count (LFCT)

The Lost Frame Count is described in the FDDI MAC standard, and is the count of all instances where a format error is detected in a frame or token such that the credibility of reception is placed in doubt. The Lost Frame Count is incremented when any symbol other than data or Idle symbols is received between the Starting and Ending Delimiters of a frame (this includes parity errors).

4.3.4 Frame Copied Count (FCCT)

The Frame Copied Count is described in the FDDI MAC standard, and is the count of the number of frames addressed to and copied by this station. The count is incremented when an internal or external match occurs (when Option.EMIND enabled) on the Destination Address, no errors were detected in the frame and the frame was successfully copied (which the Service Engine communicates to the Ring Engine via the internal VCOPY signal). Frames copied promiscuously, MAC frames, Void frames and NSA frames received with the A indicator set are not included in this count.

4.0 FDDI MAC Facilities (Continued)

4.3.5 Frames Not Copied Count (FNCT)

The Frames Not Copied Count is specified in the FDDI MAC standard, and is the count of frames intended for this station that were not successfully copied by this station. The count is incremented when an internal or external (when Option.EMIND is enabled) Destination Address match occurs, no errors were detected in the frame, and the frame was not successfully copied (VCOPY = 0). MAC frames, Void frames, and NSA frames received with the A indicator set are not included in this count.

4.3.6 Frames Transmitted Count (FTCT)

The Frames Transmitted Count is specified in the FDDI MAC standard, and is incremented every time a complete frame is transmitted from the MAC Request Interface. Void and MAC frames generated by the Ring Engine are not included in the count.

4.4 TIMERS

4.4.1 Token Rotation Timer (TRT)

The Token Rotation Timer (TRT) times token rotations from arrival to arrival. TRT is used to control ring scheduling during normal operation and to detect and recover from serious ring error situations.

TRT is loaded with the maximum token rotation time, TMAX, when the ring is not operational. TRT is loaded with the negotiated Target Token Rotation Time, TNEG, when the ring is operational.

4.4.2 Token Holding Timer (THT)

The Token Holding Timer is used to limit the amount of ring bandwidth used by a station for asynchronous traffic once the token is captured. THT is used to determine if the captured token is (still) usable for asynchronous transmission. A token is usable for asynchronous traffic if THT has not reached the selected threshold. Two asynchronous thresholds are supported; one that is fixed at the Negotiated Target Token Rotation Time (TNEG), and one that is programmable at one of 16 Asynchronous Priority Thresholds. Requests to transmit frames at one of the priority thresholds are serviced when the Token Holding Timer (THT) has not reached the selected threshold.

4.4.3 Late Count (LTCT)

The Late Count is implemented differently than suggested by the MAC standard, but provides similar information. The function of the Late Count is divided between the Late_Flag that is equivalent to the MAC standard Late Count with a non-zero value and a separate counter. Late_Flag is maintained by the Ring Engine to indicate if it is possible to send asynchronous traffic. When the ring is operational, Late Count indicates the time it took the ring to recover the last time the ring became non-operational. When the ring is non-operational, Late Count indicates the time it has taken (so far) to recover the ring.

The Late Count is incremented every time TRT expires while the ring is non-operational and Late_Flag is set (once every TMAX).

The Late Count is provided to assist Station Management, SMT, in the isolation of serious ring errors. In many situations the ring will recover very quickly and late count will be of marginal utility. However, in the case of serious ring errors, it is helpful for SMT to know how long it has been since the ring became non-operational (with TMAX resolution) in order to determine if it is necessary to invoke recovery procedures. When the ring becomes non-operational, there is no way to know how long it will stay non-operational. Therefore, a timer is necessary. If the Late Count were not provided, SMT would be forced to start a timer every time the ring becomes non-operational even though it may seldom be used. By using the provided Late Count, an SMT implementation may be able to alleviate this additional overhead.

4.4.4 Valid Transmission Timer (TVX)

The Valid Transmission Timer (TVX) is reset every time a valid frame or token is received. TVX is used to increase the responsiveness of the ring to errors. Expiration of the TVX indicates that no frame or token has been received within the timeout period and causes the Transmitter to invoke the recovery (Claim) process.

The Value of TVX is also used as the Duplicate MAC frame detection delay, DM_MIN. This is the time after which a MAC frame will be suspected as being generated by another station with this station's address when the ring is non-operational.

4.4.5 Token Received Count (TKCT)

The Token Received Count is incremented every time a valid token arrives. The Token Count can be used with the Ring Latency Count to calculate the average network load over a period of time. The frequency of token arrival is inversely related to the network load.

4.4.6 Ring Latency Count (RLCT)

The Ring Latency Count is a measurement of time for frames to propagate around the ring. This counter contains the last measured ring latency whenever the Ring Latency Valid bit of the Token Event Register (TELR0.RLVLD) is One.

The Latency Counter increments every 16 byte times (1.28 μs) and is used to measure ring latencies up to 1.3421772 seconds directly with accuracy of 1.2 μs. No overflow or increment event is provided with this counter.

4.5 RING SCHEDULING

FDDI uses a timed token protocol to schedule use of the ring. The protocol measures load on the network by timing the rotation of the token. The longer the token rotation time the greater the instantaneous load on the network. By limiting the transmission of data when the token rotation time exceeds a target rotation time, a maximum average token rotation time is realized. The protocol is used to provide different classes of service.

Multiple classes of service can be accommodated by setting different target token rotation times for each class of service.

The Ring Engine supports Synchronous, Non-restricted Asynchronous, Restricted Asynchronous, and Immediate service classes. The Immediate service class is supported when the ring is non-operational; the other classes are supported when the ring is operational.

4.5.1 Synchronous Service Class

The Synchronous Service Class may be used to guarantee a maximum response time (2 times TTRT), minimum bandwidth, or both.

4.0 FDDI MAC Facilities (Continued)

Each time the token arrives, a station is permitted to transmit one or more frames in accordance with its synchronous bandwidth allocation regardless of the status of the token (late or early; Restricted or Non-Restricted).

Since the Ring Engine does not provide a mechanism for monitoring a station's synchronous bandwidth utilization, the user must insure that no synchronous request requires more than the allocated bandwidth.

To help ensure that synchronous bandwidth is properly allocated after ring configuration, synchronous requests are not serviced after a Beacon frame is received. After a major reconfiguration has occurred, management software must intervene to verify or modify the current synchronous bandwidth allocation.

4.5.2 Non-Restricted Asynchronous Service Class

The Non-Restricted Asynchronous service class is typically used with interactive and background traffic. Non-Restricted Asynchronous requests are serviced only if the token is early and the Token Holding Timer has not reached the selected threshold.

Asynchronous service is available at two priority thresholds, the Negotiated Target Token Rotation Time plus one programmable threshold. Management software may use the priority thresholds to discriminate additional classes of traffic based on current loading characteristics of the ring. The priority thresholds may be determined using the current TTRT and the Ring Latency. In this case, application software is only concerned with the priority level of a request.

As an option, Asynchronous Requests may be serviced with THT disabled. This is useful when it is necessary to guarantee that a multi-frame request will be serviced on a single token opportunity. Because of the possibility of causing late tokens, this capability should be used with caution, and should only be allowed when absolutely necessary.

4.5.3 Restricted Asynchronous Service Class

The Restricted Asynchronous service class is useful for large transfers requiring all of the available Asynchronous bandwidth. The Restricted Token service is useful for large transfers requiring all of the available (remaining) asynchronous bandwidth.

The Restricted Token service may also be used for operations requiring instantaneous allocation of the remaining synchronous bandwidth when Restricted Requests are serviced with THT disabled. This is useful when it is necessary to guarantee atomicity, i.e., that a multi-frame request will be serviced on a single token opportunity.

A Restricted dialogue consists of three phases:

1. Initiation of a Restricted dialogue:
   - Capture a Non-restricted Token
   - Transmit zero or more frames to establish a Restricted dialogue with other stations
   - Issue a Restricted Token to allow other stations in the dialogue to transmit frames
2. Continuation of a Restricted dialogue:
   - Capture a Restricted Token
   - Transmit zero or more frames to continue the Restricted dialogue
   - Issue a Restricted Token to allow other stations in the dialogue to transmit frames
3. Termination of a Restricted dialogue:
   - Capture a Restricted Token
   - Transmit zero or more frames to continue the Restricted dialogue
   - Issue a Non-Restricted Token to return to the Non-Restricted service class

Initiation of a Restricted dialogue will prevent all Non-Restricted Asynchronous traffic throughout the ring for the duration of the dialogue, but will not affect Synchronous traffic.

To ensure that the Restricted traffic is operating properly, it is possible to monitor the use of Restricted Tokens on the ring. When a Restricted Token is received, the event is latched and, under program control, may generate an interrupt. In addition, a request to begin a Restricted dialogue will only be honored if both the previous transmitted Token and the current received Token were Non-Restricted tokens. This is to ensure that the upper bound on the presence of a Restricted dialogue in the ring is limited to a single dialogue.

As suggested by the MAC-2 standard, to help ensure that only one Restricted dialogue will be in progress at any given time, Restricted Requests are not serviced after a MAC frame is received until Restricted Requests are explicitly enabled by management software. Since the Claim process results in the generation of a Non-restricted Token, this prevents stations from initiating another restricted dialogue without the intervention of management software.

4.5.4 Immediate Service Class

The Immediate Service Class facilitates several non-standard applications and is useful in ring failure recovery (e.g., Transmission of Directed Beacons). Certain ring failures may cause the ring to be unusable for normal traffic, until the failure is remedied.

Immediate requests are only serviced when the ring is non-operational. Immediate requests may be serviced from the Transmitter Data, Claim, and Beacon States. Options are available to force the Ring Engine to enter the Claim or Beacon State, to prohibit it from entering the Claim State, or to remain in the Claim State when receiving My_Claim.

On the completion of an Immediate request, a Token (Non-restricted or Restricted) may optionally be issued. Immediate requests may also be used in non-standard applications such as a full duplex point to point link.

5.0 Functional Description (Ring Engine)

5.1 TOKEN HANDLING

5.1.1 Token Timing Logic

The FDDI Ring operates based on the Timed Token Rotation protocol where all stations on the ring negotiate for the maximum time that the stations have to wait before being able to transmit frames. This value is termed the Negotiated Target Token Rotation Time (TTRT). The TTRT value is stored in the TNEG Register.

Stations negotiate for TTRT based on their TREQ that is assigned to them upon initialization.

Each station keeps track of the token arrival by setting the Token Rotation Timer (TRT) to the TTRT value. If the token

is not received within TTRT (the token is late), the event is recorded by setting the Late_Flag. If the token is not received within twice TTRT (TRT expires and Late_Flag is set), there is a potential problem in the ring and the recovery process is invoked.

Furthermore, the Token Holding Timer (THT) is used to limit the amount of ring bandwidth used by a station for asynchronous traffic once the token is captured. Asynchronous traffic is prioritized based on the Late_Flag which denotes a threshold at TTRT and an additional Asynchronous Priority Threshold (THSH). The Asynchronous Threshold comparison (Apri 1) is pipelined, so a threshold crossing may not be detected immediately; however, the possible error is a fraction of the precision of the threshold values.

The Token Timing Logic consists of two Timers, TRT and THT, in addition to the TMAX and TNEG values loaded into these counters (see *Figure 5-1*).

The Timers are implemented as count-up counters that can increment every 80 ns. The Timers are reset by loading TNEG or TMAX into the counters where TNEG and TMAX are unsigned two's complement numbers. This allows a Carry flag to denote timer expiration.

On an early token arrival (Late_Flag is not set), TRT is loaded with TNEG and counts up. On a late token arrival (Late_Flag is set), Late_Flag is cleared and TRT continues to count. When TRT expires and Late_Flag is not set, Late_Flag is set and TRT is loaded with TNEG.

THT follows the value of TRT until a token is captured. When a token is captured, TRT may be reloaded with TNEG while THT continues to count from its previous value (THT does not wrap around). THT increments when enabled. THT is disabled during synchronous transmission and a special class of asynchronous transmission. THT is used to determine if the token is usable for asynchronous requests. For these purposes, the token is considered late one byte before it is actually late (to promote interoperability with less careful implementations).

If TRT expires while Late_Flag is set, TRT is loaded with TMAX and the recovery process (Claim) is invoked (unless the Inhibit Recovery Required option is set). The Recovery Required condition becomes true one byte time after TRT expires (to promote interoperability with less careful implementations). When TRT expires and the ring is not operational, TRT is loaded with TMAX. TRT is also loaded with TMAX on a MAC Reset.

5.1.2 Token Recovery

While the ring is operational, every station in the ring uses the Negotiated Target Token Rotation Time, TNEG. The MAC implements the protocol for negotiation of this target token rotation time (TTRT) through the Claim process. The shortest requested token rotation time is used by all of the stations in the ring as the TNEG.

If TRT expires with Late_Flag set, a token has not been received within twice TTRT (Target Token Rotation Time). If TVX (Valid Transmission Timer) expires, the station has not received a valid token within TVX Max. Both these events require token recovery and cause the Ring Engine to enter the Claim process.

In the Claim process, a MAC continuously transmits Claim frames containing TREQ. Should the MAC receive a Claim frame with a shorter TREQ (larger value—Higher_Claim) it leaves the Claim State. A station that receives its own Claim frame gains the right to send the first token and make the ring operational again. If the Claim Process does not complete successfully, TRT will expire and the Beacon Process is invoked.

The Beacon Process is used for fault isolation. A station may invoke the Beacon Process through an SM_Control.request(Beacon). When a station enters the Beacon Process, it continuously sends out Beacon Frames. The Beacon Process is complete when a station receives its own Beacon Frame. That station then enters the Claim process, to re-initialize the ring.

5.2 SERVICING TRANSMISSION REQUESTS

A Request to transmit one or more frames is serviced by the Ring Engine. After a Request is submitted to the Ring Engine, the Ring Engine awaits an appropriate Service Opportunity in which to service the Request. Frames associated with the Request are transmitted during the Service Opportunity. The definition of a Service Opportunity is different depending on the operational state of the ring.

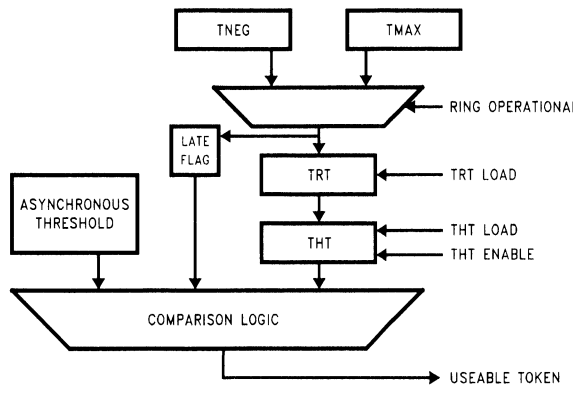


FIGURE 5-1. Token Timing Logic

5.0 Functional Description (Ring Engine) (Continued)

A Service Opportunity begins when the criteria presented to the Ring Engine are met. This criteria contains the requested service class (sync, async, async priority, immediate) and the type of token to capture (restricted, non-restricted, any, none).

During a service opportunity, the Ring Engine guarantees that a valid frame is sent with at most 40 bytes of preamble (unless Option.IRPT is set). When data is not ready to be transmitted, Void frames are transmitted to reset the TVX timers in all stations. During an immediate request from the Claim or Beacon state, if the data for external Claim or Beacon frame is not ready to be transmitted, the Ring Engine will transmit Claim or Beacon frames using the same internal data used for normal Claim and Beacon processing.

5.2.1 Service Opportunity while Ring Operational

Beginning of Service Opportunity

Table 5-1 shows the conditions that must be true when a valid token is received in order to begin a service opportunity when the ring is operational.

In addition to the criteria mentioned above, additional criteria apply to the servicing of Synchronous and Restricted Requests.

- Synchronous Requests are not serviced if MODE2.ERSTR = 0 or RELR.BCNR = 1 (see Section 4.5.1).
- Restricted requests are not serviced when MODE2.ESYNR = 0 or RELR.MACR = 1. (see Section 4.5.3).
- Restricted Dialogues may only begin when a non-restricted token has been received and transmitted (see Section 4.5.3).

End of Service Opportunity

The Service Opportunity continues until either a token is issued or the ring becomes non-operational.

A token is issued after the current frame, if any, is transmitted when:

1. It is no longer necessary to hold the token
   - All frames of all active requests have been transmitted
2. The token became unusable while servicing a request
   - Asynchronous Priority threshold reached (if an Async Priority Request is being serviced)
   - THT expired (if enabled)

When the ring becomes non-operational the current frame transmission is aborted. The ring may go non-operational while holding a token as a result of any one of the following conditions being present:

- A MAC Reset
- Reception of a valid MAC frame
- TRT expiration (TRT was reset when the token was captured)

Issue Token Type

The criteria presented to the Ring Engine to begin a service opportunity also contains the Issue Token Class. The Issue Token Class is used if servicing of that request was completed (the last frame of that request was transmitted). Otherwise, a token of the capture token class is issued.

TABLE 5-1. Beginning of Service Opportunity

Requested Service Class	Requested Token Capture Class	Criteria	Received Token Class
Asynchronous Priority	non-restricted	THT > THSH Late_Flag = 0 Ring_Op = 1	non-restricted
Asynchronous	non-restricted	Late_Flag = 0 Ring_Op = 1	non-restricted
Asynchronous	restricted	Late_Flag = 0 Ring_Op = 1	restricted
Synchronous	any	Ring_Op = 1	any

When servicing multiple requests on a single service opportunity, the issue token class of the previous class becomes the capture class for the next request for purposes of determining usability.

The type of token issued depends on the service class and the type of token captured as shown in Table 5-2.

5.2.2 Service Opportunity While Ring Not Operational

While the ring is not operational, a service opportunity occurs if an immediate transmission is requested from the transmitter Data, Claim or Beacon state, and the transmitter is in the appropriate state.

The service opportunity continues until any one of the following conditions exist:

1. No (additional) frames are to be sent
2. Time TMAX elapses on this request
3. The transmitter exits the requested state
4. The ring becomes operational while servicing an immediate request

5.2.3 Frame Transmission

Frames associated with the current request may be transmitted at any time during a Service Opportunity. In many applications, data is ready to be transmitted when the Request is presented to the interface. Soon after the Service Opportunity begins, frame transmission begins. In other applications, in order to minimize the effects of ring latency, it is desirable to capture the token when no data is ready to be transmitted. This capability results in wasted ring bandwidth and should be used judiciously.

During transmission, a byte stream is passed from the System Interface to the MAC Request Interface. The data is passed through the Ring Engine and appears at the PHY Request Interface two byte times later.

While a frame is being transmitted, the Request parameters for the next Request (if different) may be presented to the interface. At the end of the current frame transmission, a decision is made to continue or cancel the current service opportunity based on the new Request parameters.

Several errors can occur during a transmission. A transmission may be terminated unsuccessfully because of external buffering or interface parity errors, internal Ring Engine errors, a MAC reset, or reception of a MAC frame. When a

transmission is aborted due to an external error (and Option.IRPT is not set), a Void frame is transmitted to reset the TVX timers in all stations in the ring. When a frame is aborted due to a transmission error, the service opportunity is not automatically ended.

5.3 REQUEST SERVICE PARAMETERS

5.3.1 Request Service Class

The Requested Service corresponds to the Request Service Class and the Token Class parameters of the (SM__)MA__DATA.request and (SM__)MA__Token.request primitives as specified in the Standard.

TABLE 5-2. Token Transmission Type

Service Class	Token Captured	Token Issued
Non-restricted	Non-restricted	Non-restricted
Begin Restricted	Non-restricted	Restricted
Continue Restricted	Restricted	Restricted
End Restricted	Restricted	Non-restricted
Immediate	None	None
Immediate Non-restricted	None	Non-restricted
Immediate Restricted	None	Restricted

14 useful combinations of the requested Service Class (Non-Restricted Asynchronous, Restricted Asynchronous, Synchronous, Immediate), the Token Capture and Issue Class, and THT Enable are supported by the Ring Engine as shown in Table 5-3.

Requests are serviced on a Service Opportunity meeting the requested criteria.

A Token Capture Class of **non-rstr** indicates that the Transmitter Token Class must be Non-Restricted to begin servicing the request. A Token Capture Class of **rstr** indicates that the Transmitter Token Class must be Restricted to begin servicing the Request. A Token Issue Class of **non-rstr** means that the Transmitter Token Class will be Non-restricted upon completion of the request. A Token Issue Class of **rstr** means that the Transmitter Token Class will be Restricted upon completion of the request.

5.3.2 Request Options

The Request options provide the ability for Source Address Transparency (SAT) and FCS Transparency (FCST). In both cases, data from the request stream is transmitted in place of data from the Ring Engine. The use of Source Address Transparency has no effect on the sequencing of the interface. When Source Address transparency is not used, the SA from the internal parameter RAM is substituted for the SA bytes in the request stream, which must still be present. Since the FCS is appended to the frame, when FCS transparency is not used, no FCS bytes are present in the request stream.

Source Address Transparency (SAT)

Normally, the SA field in a frame is generated by the Ring Engine using either the MSA or MLA values programmed in the parameter RAM. When the SA Transparency option is selected, the SA from the data stream is transmitted in place of the MSA or MLA. The SAT option can be invoked on a Request Object via the Request Configuration parameters of the System Interface.

When the SA Transparency option is selected, it is necessary to rely on an alternate stripping mechanism since stripping based on the returning SA only guarantees that frames with MSA or MLA will be stripped. Either the Void Stripping option (described below) may be invoked, or external hardware that forces stripping using the EM (External M__Flag) signal is required.

The MSB of the SA is not controlled by this option. It is normally forced to Zero. It can be controlled using the Source Address MSB Transparency option described below.

SA Transparency is possible for all frames (including MAC frames). External support is required to limit the use of SA Transparency to certain MAC Users. SA Transparency should not be used with externally generated MAC Frames in order to maintain accountability, but this is not enforced by the Ring Engine. When SA Transparency is used with externally generated Beacon Frames that are transmitted from the Beacon state, the first 4 bytes of the INFO field are passed transparently from the data stream instead of being generated by the Ring Engine.

SA Transparency also overrides the Long and Short Addressing enables. For example, if Long Addressing is not enabled, it is still possible to transmit frames with Long Addresses. Similarly, if Short Addressing is not enabled, it is still possible to transmit Frames with Short Addresses. This may be useful in full duplex point to point applications and for diagnostic purposes.

Source Address Most Significant Bit Transparency

With the Source Address MSB Transparency option, the MSB of the SA is sourced from the data stream, as opposed to being transmitted as Zero. The SA MSB Transparency option is selected through the Request Channel Configuration Registers in the Service Engine.

Unless the Source Address Transparency option is also selected, the rest of the SA is generated by the Ring Engine.

The MSB of the SA is used to denote the presence of the Routing Information Field used in Source Routing algorithms (as in the IEEE 802.5 protocol). This option is useful for stations that use Source Routing. In these applications, the SA can still be generated by the Ring Engine, even when routing information is inserted into the data stream. This allows the normal stripping to be accomplished in end stations implementing Source Routing (without relying on external software to not create no-owner frames).

Void Stripping

This option is useful for removing bridged and ownerless frames and remnants (fragments) from the ring.

In the Void Stripping protocol, two My__Void frames are transmitted at the end of a service opportunity. Stripping continues until one of the following conditions occur:

- One My__Void frame returns (The Second My__Void will be stripped on the basis of the SA)
- A Token is received
- An Other__Void is received
- A MAC frame other than My__Claim is received
- A MAC Reset occurs

If any frame of a service opportunity requests this option, then all frames on that service opportunity will be stripped using this method. Void Stripping is invoked upon the assertion of the STRIP signal at the beginning of a frame transmission.

Void Stripping is also automatically invoked by this station if it wins the Claim token process before the initial token is issued. This removes all fragments and ownerless frames from the ring when the ring becomes operational.

FCS Transparency

Normally, the Ring Engine generates and transmits the FCS. When the Frame Check Sequence Transparency option is selected, the Ring Engine device does not append the FCS to the end of the Information field. This option is selected by asserting signal FCST.

The receiving stations treat the last four bytes of the data stream as the FCS.

This option may be useful for end to end FCS coverage when crossing FDDI bridges, for diagnostic purposes, or in Implementer frames.

5.4 FRAME VALIDITY PROCESSING

A valid frame is a frame that meets the minimum length criteria and contains an integral number of data symbol pairs between the Starting and Ending Delimiters as shown in Table 5-4.

TABLE 5-3. Request Service Classes

RQRCLS	Name	Class	THT	Token Capture	Token Issue	Notes
0000	None	None				
0001	Apri_1	Async THSH1	enabled	non-rstr	non-rstr	
0010	Reserved	Reserved				
0011	Reserved	Reserved				
0100	Sync	Sync	disabled	any	captured	1
0101	Imm	Immediate	disabled	none	none	4
0110	ImmN	Immediate	disabled	none	non-rstr	4
0111	ImmR	Immediate	disabled	none	rstr	4
1000	Async	Async	enabled	non-rstr	non-rstr	
1001	Rbeg	Restricted	enabled	non-rstr	rstr	2, 3
1010	Rend	Restricted	enabled	rstr	non-rstr	2
1011	Rcnt	Restricted	enabled	rstr	rstr	2
1100	AsynD	Async	disabled	non-rstr	non-rstr	
1101	RbeginD	Restricted	disabled	non-rstr	rstr	2, 3
1110	RendD	Restricted	disabled	rstr	non-rstr	2
1111	RcntD	Restricted	disabled	rstr	rstr	2

Note 1: Synchronous Requests are not serviced when MODE1.ESYNR = 0 or RELR.BCNR = 1.

Note 2: Restricted Requests are not serviced when MODE1.ERSTR = 0 or RELR.MACR = 1.

Note 3: Restricted Dialogues only begin when a Non-Restricted token has been received and transmitted.

Note 4: Immediate Requests are serviced when the ring is Non-Operational. These requests are serviced from the Data state if neither signal RQCLM nor RQBCN is asserted. If signal RQCLM is asserted, Immediate Requests are serviced from the Claim State. If signal RQBCN is asserted, Immediate Requests are serviced from the Beacon State. RQCLM and RQBCN do not cause transitions to the Claim and Beacon States.

On Transmit, frames are checked to see that they are of a minimum length. If the end of a frame is reached before a valid length is transmitted, the frame will be aborted and a Void frame will be transmitted (as with all aborted frames). A MAC frame with a zero length INFO field will not be aborted even though the Receiver will not recognize it as a valid frame. Frame lengths are not checked for the maximum allowable length (4500 bytes).

TABLE 5-4. Valid Frame Length

Frame Types	Short Address	Long Address	Notes
	(minimum number of bytes)		
Void	9	17	
MAC	13	21	including a 4 byte INFO field
non-MAC	9	17	including a 0 byte INFO field

Also on the Transmit side, the L bit in the FC field is checked against the ESA and ELA bits in the Option Register (if the SA Transparency option is not selected) to insure that a frame of that address length can be transmitted. If the selected address length is not enabled, the frame is aborted at the beginning of the SA field. If SA Transparency is selected, the frame is not aborted.

When Option.IRPT is set and SAT and SAIGT are selected or when Mode.DIAG is set, the minimum frame length is one data byte.

5.5 FRAME STATUS PROCESSING

Each frame contains three or more Control Indicators. The FDDI Standard specifies three: the E, A, and C Indicators.

When a frame is transmitted, the Control Indicators are transmitted as R (Reset) symbols. If an error is detected by a station that receives the frame, the E Indicator is changed to an S (Set) symbol. If a station recognizes the DA of a frame as its own address (Individual, Group, or Broadcast), the A Indicator is changed to an S symbol. If that station then copies the frame, the C Indicator is changed to an S symbol.

The received value of the Control Indicators for every frame received is reported at the MAC Indicate Interface on signals MID(7–0). On a frame transmitted by this station, the returning Control Indicators give the transmission status.

5.0 Functional Description (Ring Engine) (Continued)

The Ending Delimiter followed by the Frame Status Indicators should begin and end on byte boundaries. Control Indicators are repeated until the first non R, S, or T symbol is received.

The processing of properly aligned E, A and C indicators by the Ring Engine is detailed in Table 5-5. Given the shown received Control Indicator values and the settings of the internal flags, the noted control indicator values will be transmitted.

5.5.1 Odd Symbols Handling

When the first T symbol of a frame is received as the second symbol of a symbol pair (the T symbol is received off-boundary), the Ring Engine signals this condition by sending out the symbol sequence TSII. This indicates the end of frame for a frame which had an error. Note that this is a low probability error event.

Reception of symbols other than R, S, or T during the Frame Status processing is also a low probability event.

5.6 SMT FRAME PROCESSING

All SMT frames are handled as all other frames with the exception of the SMT Next Station Addressing (SMT NSA) frame. NSA frames are used to announce this station's address to the next addressed station. The current SMT protocol requires stations to periodically (at least once every 30 seconds) transmit an NSA frame. Since the Broadcast address is used, and every station is required to recognize the broadcast address, the downstream neighbor will set the A Indicator. A station can determine its upstream neighbor by finding NSA frames received with the A Indicator received as R. By collecting this information from all stations, a map of the logical ring can be built.

TABLE 5-5. Control Indicator Processing

Received Indicators			Flags				Transmitted Indicators		
E	A	C	E	A	Copy	N	E	A	C
R	R	R	0	0	X	X	R	R	R
R	R	R	0	1	0	X	R	S	R
R	R	R	0	1	1	X	R	S	S
X	R	R	1	X	X	X	S	R	R
R	R	S	0	0	X	X	R	R	S
R	R	S	0	1	0	X	R	S	R
R	R	S	0	1	1	X	R	S	S
X	R	S	1	X	X	X	S	R	S
R	S	R	0	X	X	1	R	S	R
R	S	R	0	X	0	0	R	S	R
R	S	R	0	1	1	0	R	S	R
R	S	R	0	0	X	X	R	S	S
R	S	S	0	X	X	X	R	S	S
X	S	S	1	X	X	X	S	S	S
R	R	T	0	0	X	X	R	R	T
R	R	T	0	1	0	X	R	S	R
R	R	T	0	1	1	X	R	S	S
X	R	T	1	X	X	X	S	R	T
R	S	T	0	1	1	0	R	S	S
R	S	T	0	0	X	X	R	S	T
R	S	T	0	1	0	X	R	S	R
R	S	T	0	1	1	1	R	S	R
X	S	T	1	X	X	X	S	S	T

E_Flag is set when the local FCS check fails or when the E Indicator is received as anything other than R.

A_Flag is the value of the internal A_Flag or the external A_Flag as indicated by the EA input signal (when Option.Emind is set).

EC represents the value of the External C indicator Input Signal one byte time before then ending delimiter of the frame.

The Copy Flag is a one cycle delayed version of the VCOPY input.

N_Flag indicates that an NSA frame is being received. This signal is sampled at the same time that the received A indicator is being investigated.

X Represents a Don't Care Condition.

5.0 Functional Description (Ring Engine) (Continued)

Additionally, only the station that sets the A Indicator is permitted to set the C Indicator on such frames. In this way, the station that sends out the NSA frame can determine if the next addressed station copied the frame by examining the returning C Indicator.

5.7 MAC FRAME PROCESSING

Upon the reception of a valid MAC frame (Claim, Beacon, or Other), the Ring_Operational flag is reset and the Ring Engine enters the Idle, Claim or Beacon State. Received Claim and Beacon frames are processed as defined in the MAC Standard, unless explicitly inhibited by the bits in the Option Register (e.g., Inhibit Recovery Required).

5.7.1 Claim Token Process

Receive

When a Claim frame is received, its Frame Type is reported (Claim frame) along with the type of Claim frame.

There are three types of Claim frames: My_Claim, Higher_Claim, and Lower_Claim.

A My_Claim frame is a Claim frame with a Source Address that matches this station address and the T_Bid_Rc in the INFO field is equal to this station's TREQ.

A Higher_Claim frame is a Claim frame with a Source Address that does not match this station address and the T_Bid_Rc in the INFO field is greater than this station's TREQ.

A Lower_Claim frame is a Claim frame with a Source Address that does not match this station address and the T_Bid_Rc in the INFO field is smaller than this station's TREQ.

Transmit

Claim frames are transmitted continuously while in the Tx_Claim State.

Claim frames are generated by the Ring Engine unless an Immediate Claim Request is present at the MAC Request Interface. Even if an Immediate Claim Request is present at the MAC Request Interface, at least one Claim frame must be generated by the Ring Engine before Claim frames from the Interface are transmitted.

For internally generated Claim frames, the Information field is transmitted as the 4-byte Requested Target Token Rotation Time.

The Information field of a Claim frame consists of this station's Requested Target Token Rotation Time. In the Ring Engine implementation, TREQ is programmable with a 20.48 μs resolution and a maximum value of 1.34 seconds.

Claim Protocol

Entry to the Tx_Claim state occurs whenever token recovery is required. The Recovery Required condition occurs when:

- TRT expires and Late_Flag is set
- TVX expires
- A Lower Claim frame or My_Beacon frame is received

Entry to the TX_Claim state may be blocked by enabling the Inhibit Recovery Required option (bit Option.IRR).

The Tx_Claim state is entered (even if Option.IRR = 1) with an SM_MA_Control.request(Claim) which is accomplished by setting Function.CLM to 1.

While in the Tx_Claim state:

- Claim frames are transmitted continuously
- If a Higher_Claim frame is received, the station exits the Claim state and enters the IDLE state. In this state it then repeats additional Higher_Claim frames.
- If a Lower_Claim frame is received, this station continues to send its own Claim frames and remains in the Claim state.

Eventually, if a logical ring exists, the station with the shortest TREQ on the ring should receive its own Claim frames, the My_Claim frame. This completes the Claim Token Process. This one station then earns the right to issue a token to establish an Operational ring.

An option is provided to remain in the Claim state if this station won the Claim Token Process by enabling the Inhibit Token Release Option (bit Option.IRR).

5.7.2 Beacon Process

Receive

When a Beacon frame is received, its Frame Type is reported (Beacon frame) along with the type of Beacon frame.

There are two types of Beacon frames: My_Beacon and Other_Beacon.

A Beacon frame is considered a My_Beacon if its Source Address matches this station's address (long or short).

A Beacon frame is marked as Other_Beacon if its Source Address does not match this station's address.

Transmit

Beacon frames are transmitted continuously while in the Tx_Beacon state.

Beacon frames are generated by the Ring Engine, unless an Immediate Beacon Request is present at the MAC Request Interface. Even if an Immediate Beacon Request is present at the MAC Request Interface, at least one Beacon frame must be generated by the Ring Engine before Beacon frames from the Interface are transmitted.

For internally generated Beacon frames, the Ring Engine uses the TBT in the Information field.

Beacon Protocol

Entry to the Tx_Beacon state occurs under two conditions:

- A failed Claim Process (TRT expires during the Claim process)
- An SM_MA_Control.request(Beacon) which is accomplished by setting Function.BCN to 1).

Beacon frames are then transmitted until the Beacon process is completed.

If an Other_Beacon frame is received, this station exits the Beacon state, stops sending its own Beacon frames, and repeats the incoming Beacon frames.

If a My_Beacon frame is received, the station has received back its own Beacon frame; thus successfully completing the Beacon process. The station then enters the Claim Process.

5.7.3 Handling Reserved MAC Frames

A Reserved MAC frame is any MAC frame aside from Beacon and Claim frames. Tokens are not considered MAC frames even though their Format bit (FC.FF) is the same as for MAC frames.

When a Reserved MAC frame (Other_MAC) is received, it is treated as a Higher Claim. If the Transmitter is in the Claim state when a Reserved MAC frame is received, the Transmitter returns to the Idle state and then repeats the next Reserved MAC frame received. If the Transmitter is in the Beacon state and a Reserved MAC frame is received, the Transmitter continues to transmit Beacon frames. If the Transmitter is in the Idle state, the Reserved MAC frame is repeated.

5.8 RECEIVE BATCHING SUPPORT

The Ring Engine stores each received SA and compares the incoming SA with the previous SA. This may be used to batch status on frames received from the same station.

The SameSA signal is asserted when:

1. The current and previous non-Void frames were not MAC frames.
2. The size of the address of the current frame is the same as the size of the address of the previous non-Void frame.
3. The SA of the current frame is the same as the SA of the previous non-Void frame.

On MAC frames, the Information fields are compared. This information may be useful to inhibit copying MAC frames with identical information. This is particularly useful for copying Claim and Beacon frames when new information is present.

The Same INFO signal is asserted when:

1. The current and previous non-Void frames were both MAC frames (not necessarily the same FC value).
2. The first four bytes of the INFO field of the current frame is the same as the first four bytes of the INFO field of the previous non-Void frame.

The size of the address of MAC frames is not checked.

5.9 IMMEDIATE FRAME TRANSMISSION

Immediate requests are used when it is desirable to send frames without first capturing a token. Immediate requests are typically used as part of management processes for Error Isolation and Recovery. Immediate requests are also useful in full duplex applications. Immediate requests are serviced only when the station's Ring_Operational flag is Zero (CTSR.ROP = 0).

To transmit an Immediate request, the request must first be queued at the MA_Request Interface. If the Ring is not operational (Ring_Operational flag is not set), the request will be serviced immediately. If the Ring is operational (Ring_Operational flag is set), the request will be serviced when the Ring becomes non-operational. The Ring becomes non-operational as a result of a MAC Reset (Function.MCRST is set to One) or any of the conditions causing the Reset or Recovery Actions to be performed.

In addition to servicing an Immediate request from the Tx_Data State, it is also possible to service Immediate requests from the Tx_Claim or Tx_Beacon State. When transmitting from the Claim or Beacon state, in addition to requesting an Immediate Transmission Service Class, the RQCLM or RQBCN signals must be asserted to indicate an Immediate Claim or Immediate Beacon request. These requests will only be serviced when in the Claim or Beacon state. Entry to the Tx_Beacon State can be forced by setting bit BCN of the Function Register to One. Entry to the Tx_Claim State can be forced by setting bit CLM of the Function Register to One.

While in the Tx_Claim or Tx_Beacon state, the Ring Engine will transmit internally generated Claim or Beacon frames except when an Immediate Claim or Beacon request is present at the MA_Request Interface, signal RQCLM or RQBCN is asserted, and a frame is ready to be transmitted. At least one internally generated Claim or Beacon frame must be transmitted before an Immediate Claim or Beacon request is serviced. It is possible for the internally generated frame to return before the end of the requested frame has been transmitted. To allow time for the requested frame(s) to be transmitted before leaving the Claim or Beacon state, bit ITR (for Claim) or bit IRR (for Beacon) of the Option Register should be set to One.

While an Immediate request is being serviced (from any state), if bit IRPT of the Option Register is set to One (Inhibit Repeat option), all received frames (except Lower_Claim and My_Beacon frames) are ignored and the Immediate request continues. Lower_Claim and My_Beacon frames can also be ignored by setting bit IRR of the Option Register.

5.10 FULL DUPLEX OPERATION

The Ring Engine supports full duplex operation by

1. Suspending the Token Management and Token Recovery protocols (set Option.IRR).
2. Inhibiting the repetition of all frames and tokens (set Option.IRPT).
3. Using the Immediate Service Class.

Frames of any size may be transmitted or received, subject to the minimum length specified in Section 5.4.

5.11 PARITY PROCESSING

Through Parity is supported on the internal data paths between any Request interface and any Indicate interface.

Odd Parity is provided every clock on all data outputs and is checked every clock on all data inputs. Parity errors are not propagated through the Ring Engine (from the MAC Request and PHY Indication interface to the PHY Request interface or from the PHY Indication interface to the MAC Indication interface). Parity errors are isolated and resolved.

When parity is not used on an Interface, the parity provided by the Ring Engine for its outputs may be ignored. For the Ring Engine's inputs, the result of the parity check is used only if parity on that Interface is enabled.

Interface parity is enabled by setting the appropriate bit in the Mode register: Mode.CBP for Control Bus Parity, Mode.PIP for PHY Indication parity and Mode.MRP for MAC Request Parity. A Master Reset (Function.MARST) disables parity on all interfaces.

5.0 Functional Description (Ring Engine) (Continued)

On the PHY Request interface, parity is generated for internally sourced fields (such as the SA or FCS on frames when not using SA or FCS transparency, and internally generated Beacon, Claim and Void frames). Odd parity is always generated for PRP. This allows through parity support at the PHY interface even if parity is not used at the MAC interface. This is very desirable since every byte of data that traverses the ring travels across the PHY Interface which is actually part of the ring.

Through parity is not supported in the Control Interface Registers and the Parameter RAM. Parity is generated and stripped at the Control Interface.

Handling Parity Errors

Parity errors are reported in the Exception Status Register when parity on that interface is enabled.

A parity error at the PHY interface (when Mode.PIP is set) is treated as a code violation and ESR.PPE is set. If the parity error occurs in the middle of token or frame reception, the token or frame is stripped, a Format Error is signalled (FOERROR) and the Lost Count is incremented.

A parity error at the MAC Interface (when Mode.MRP is set) during a frame transmission from the MAC interface (while TXACK is asserted) causes the frame transmission to be aborted. When a frame is aborted, a Void frame is transmitted to reset every station's TVX timer. A parity error (when enabled) causes ESR.MPE to be set.

A parity error at the Control Interface (when Mode.CBP is set) will cancel the current write access. ESR.CPE is set to indicate that a parity error occurred and ESR.CCE is set to indicate that the write was not performed.

5.12 HANDLING INTERNAL ERRORS

Errors internal to the Ring Engine cause a MAC Reset. This includes detecting illegal states in the state machines. Internal Errors are reported in the Internal Error Latch Register (IELR). After an internal state machine error is detected and reported (IELR.RSMERR for the receiver and IELR.TSMERR for the transmitter), the current state registers continue to be updated as always.

In diagnose mode, the Current Receive and Transmit Status Registers are frozen with the errored state until the internal state machine error condition is cleared (IELR.RSMERR and/or IELR.TSMERR).

6.0 Functional Description (Service Engine)

6.1 OVERVIEW

The Service Engine consists of two major blocks: the Indicate Machine and the Request Machine. These blocks share the Bus Interface Unit, Status/Space Machine, Pointer RAM, and Limit RAM blocks.

The Service Engine provides an interface between the Ring Engine FDDI Media Access Control Protocol block and a host system. The Service Engine transfers FDDI frames between the FDDI device and host memory.

6.1.1 Indicate Machine

On the Receive side (from the ring) the Indicate Machine sequences through the incoming byte stream from the Ring Engine. Received frames are sorted onto Indicate Channels and a decision is made whether or not to copy them to host memory. The Indicate Machine uses the control signals provided by the Ring Engine Receive State Machine on the MAC Indicate Interface to make this decision.

6.1.2 Request Machine

On the Transmit side (to the ring) the Request Machine prepares one or more frames from host memory for transmission to the Ring Engine. The Request Machine provides all the control signals to drive the Ring Engine Request Interface.

6.2 OPERATION

6.2.1 Indicate Operation

The Indicate Block accepts data from the Ring Engine as a byte stream.

Upon receiving the data, the Indicate Block performs the following functions:

- Decodes the Frame Control field to determine the frame type
- Sorts the received frames onto Channels according to the Sort Mode
- Optionally Filters identical MAC frames
- Filters Void frames
- Copies the received frames to memory according to Copy Criteria
- Writes status for the received frames to the Indicate Status Queue
- Issues interrupts to the host on host-defined status breakpoints

The Indicate Machine decodes the Frame Control (FC) field to determine the type of frame. The following types of frames are recognized: Logical Link Control (LLC), Restricted Token, Unrestricted Token, Reserved, Station Management (SMT), SMT Next Station Addressing, MAC Beacon, MAC Claim, Other MAC, and Implementer.

The Indicate Machine sorts incoming frames onto Indicate Channels according to the frame's FC field, the state of the AFLAG signal from the Ring Engine (which indicates that the MACSI device had an internal address match), and the host-defined sorting mode programmed in the Sort Mode field of the Indicate Mode Register. SMT and MAC frames are always sorted onto Indicate Channel 0. On Indicate Channels 1 and 2, frames can be sorted according to whether they are synchronous or asynchronous, or whether they are high-priority asynchronous or low-priority asynchronous. Frames can also be sorted by whether their address matches an internal (MACSI device) or external address, or based on header and Information fields for all non-MAC/SMT frames.

The Synchronous/Asynchronous Sort Mode is intended for use in end-stations or applications using synchronous transmission.

6.0 Functional Description (Service Engine) (Continued)

With High-priority/Low-priority sorting, high-priority asynchronous frames are sorted onto Indicate Channel 1 and low-priority asynchronous frames are sorted onto Indicate Channel 2. The most-significant bit of the three-bit priority field within the FC field determines the priority. This Mode is intended for end stations using two priority levels of asynchronous transmission. Synchronous frames are sorted to Indicate Channel 1 in this mode.

With External/Internal sorting, frames matching the internal address (Individual or Group addresses in the MACSI device) are sorted onto Indicate Channel 1 and frames matching an external address (when the ECOPY input is asserted) are sorted onto Indicate Channel 2. Note that under some conditions it is possible to sort internal address match and SMT/MAC frames to Indicate Channel 2. Please see Section 6.3 for full details on the External Matching Interface. This sort mode is intended for bridges or ring monitors, which would use the ECIP/ECOPY/EM pins with external address matching circuitry. However, designers should be aware of the functioning of the ECIP pin even if external matching will not be used. If ECIP is left in an improper state (e.g., floating or tied high), it will affect the operation of the MACSI device even when External/Internal sorting is not enabled.

With the Header/Info Sort Mode, Indicate Channels 1 and 2 receive all non-MAC/SMT frames that are to be copied, but between them split the frame header (whose length is user-defined) and the remaining portions of the frame (Info). Indicate Channel 1 copies the initial bytes up until the host-defined header length is reached. The remainder of the frame's bytes are copied onto Indicate Channel 2. Only one IDUD stream is produced (on Indicate Channel 1), but both Pool Space Pointer (PSP) Queues are used to determine where the IDUs will be written. When a multi-part IDUD is produced, the Indicate Status field is used to determine which parts point to the header and which point to the Info. This Mode is intended for high-performance protocol processing applications.

The Indicate Machine filters identical MAC and SMT frames when the SKIP bit in the Indicate Mode Register is set and the Indicate Configuration Register's Copy Control field (2 bits) for Indicate Channel 0 is set to 01 or 10.

Received frames are copied to memory based on the AFLAG, MFLAG, ECIP, ECOPY, and EM input signals from external address matching logic, control signals from the Ring Engine, as well as the Indicate Channel's Copy Control field. Received frames are written as a series of Input Data Units to the current Indicate memory page defined by the host via a PSP. Each frame is aligned to the start of a currently-defined burst-size memory block (16 or 32 bytes as programmed in the Mode Register's SMLB bit). The first word written contains four copies of the FC byte. The IDUD pointer points to the last FC byte so that host software sees only a single FC byte as expected. The extra FC bytes have the advantage of causing the INFO field to be aligned to a 32-bit word boundary. The format differs according to the setting of the Mode Register's BIGEND (Big Endian) bit, as shown in *Figure 6-1*.

Byte 0 **Byte 3**

Bit 31 **Big Endian Indicate Data Unit Format** **Bit 0**

FC	FC	FC	FC
DA0	DA1	SA0	SA1

Byte 3 **Byte 0**

Bit 0 **Little Endian Indicate Data Unit Format** **Bit 31**

FC	FC	FC	FC
SA1	SA0	DA1	DA0

FIGURE 6-1. Indicate Data Unit Formats (Short Address)

For each Input Data Unit, the Indicate Machine creates an Input Data Unit Descriptor (IDUD), which contains status information about the IDU, its size (byte count), and its location in memory. For IDUs that fit within the current Indicate memory page, an IDUD.Only Descriptor is created. For IDUs that span more than one memory page, a multi-part IDUD is created. For example, when a frame crosses a page boundary, the MACSI device writes an IDUD.First. If another page is crossed, an IDUD.Middle will be written. At the frame end, an IDUD.Last is written. IDUDs are written to consecutive locations in the Indicate Status Queue for the particular Indicate Channel, up to the host-defined queue limit.

The MACSI device has two modes for storing IDUs into Pool Space Pages. In the first mode, the MACSI device will assemble as many frames into a 4 kByte page as will fit. Thus, a single page of Pool Space memory may contain multiple frames and have many IDUDs pointing to it. In the second mode, the MACSI device forces a page break after the end of each frame. This means that a single page of Pool Space memory will have at most a single IDUD pointing to it. This mode greatly simplifies space reclamation in those systems which do not process incoming frames in order of receipt and supports systems in which the cache line size is greater than 32 bytes.

The Indicate Machine copies IDUs and IDUDs to memory as long as there are no exceptions or errors and the Channel has data and status space. When a lack of either data or status space is detected on a particular Channel, the Indicate Machine stops copying new frames for that Channel (only). It will set the No Status Space attention bit in the No Space Attention Register when it runs out of Status Space. It will set the Low Data Space bit in the No Space Attention Register when the last available PSP is prefetched from the Indicate Channel PSP Queue. The host allocates more data space by adding PSPs to the tail of the PSP Queue and then updating the PSP Queue Limit Register, which causes the MACSI device to clear the Low Data Space attention bit and resume copying (on the same Channel). The user should **never** clear the Low Data Space attention bits directly. The host allocates more status space by updating the IDUD Queue Limit Register and then explicitly clearing the Channel's No Status Space bit, after which the Indicate Machine resumes copying. Note that the No Status Space Attention bit must be cleared **after** the appropriate limit register is updated.

6.0 Functional Description (Service Engine) (Continued)

The MACSI device provides the ability to group incoming frames and then generate interrupts (via attentions) at group boundaries. To group incoming frames, the MACSI device defines status breakpoints, which identify the end of a group (burst) of related frames. Status breakpoints can be enabled to generate an attention.

The breakpoints for Indicate Channels are defined by the host in the Indicate Mode, Indicate Notify, and Indicate Threshold registers. Status breakpoints include Channel change, receipt of a token, SA change, DA change, MAC Info change, or a user-specified number of frames have been copied on a particular Indicate Channel.

Status breakpoint generation may be individually enabled for Indicate Channels 1 and 2 by setting the corresponding Breakpoint bits (Breakpoint on Burst End, Breakpoint on Service Opportunity, and Breakpoint on Threshold) in the Indicate Mode Register, and enabling the breakpoints to generate an attention by setting the corresponding Breakpoint bit in the Indicate Notify Register.

When an Indicate exception occurs, the current frame is marked complete, status is written into an IDUD.Last, and the Channel's Exception (EXC) bit in the Indicate Attention Register is set.

When an Indicate error (other than a parity error) is detected, the Error (ERR) bit in the State Attention Register is set. The host must reset the INSTOP Attention bit to restart processing.

When parity checking is enabled and a parity error is detected in a received frame, it is recorded in the Indicate Status field of the IDUD, and the Ring Engine Parity Error (REPE) bit in the Status Attention Register is set.

A frame which is stripped after the fourth byte of the Information Field (this may occur because an upstream station detected an error within the frame) will be copied to memory but the status will show that the frame was stripped.

6.2.2 Request Operation

The Request Block transmits frames from host memory to the Ring Engine. Data is presented to the Ring Engine as a byte stream.

The Request Block performs the following functions:

- Prioritizes active requests to transmit frames
- Requests the Ring Engine to obtain a token
- Transmits frames to the Ring Engine
- Writes status for transmitted and returning frames
- Issues interrupts to the host on user-defined group boundaries

The Request Machine processes requests by first reading Request Descriptors from the REQ Queue and then assembling frames of the specified service class, Frame Control (FC) and expected status for transmission to the Ring Engine. Request and ODUD Descriptors are checked for consistency and the Request Class is checked for compatibility with the current ring state. When an inconsistency or incompatibility is detected, the request is aborted.

When a consistency failure occurs, the Request is terminated and a Confirmation Descriptor (CNF) with the appropriate status is generated. The Request Machine then locates the end of the current object (REQ or ODUD). If the current Descriptor is not the end (Last bit not set), the Request Machine will fetch subsequent Descriptors until it detects the end and then resume processing with the next Descriptor.First or Descriptor.Only.

Requests are processed on both Request Channels simultaneously. Their interaction is determined by their priorities (Request Channel 0 has higher priority than Request Channel 1) and the Hold and Preempt/Prestage bits in the Request Channel's Request Configuration Register. An active Request Channel 0 is always serviced first, and may be programmed to preempt Request Channel 1, such that uncommitted Request Channel 1's data already in the request FIFO will be purged and then refetched after servicing Request Channel 0. When prestaging is enabled, the next frame is staged before the token arrives. Prestaging is always enabled for Request Channel 0, and is a programmable option on Request Channel 1. The MACSI device will process at most one Request per Channel per Service Opportunity.

The MACSI device contains an option bit which controls the timing of Token capture. This bit is the Early Token Request bit (ETR) which is in R0CR1 (for Request Channel 0) and R1CR1 (for Request Channel 1). When the ETR bit is disabled for a channel, the MACSI device will fetch a Request descriptor and then fetch the first ODUD and begin filling the transmit FIFO for that channel. When the FIFO threshold is reached (R0CR0.TT or R1CR0.TT) the MACSI device presents a Request Class to the Ring Engine which causes the Ring Engine to capture a Token of the specified class.

When the ETR bit is enabled, a REQ.First is loaded, the Request Machine commands the Ring Engine to capture a token of the type specified in the REQ Descriptor, and concurrently fetches the first ODUD. This mode is useful for systems which need tight control of the Token capture timing (e.g., systems using Synchronous traffic). Note that use of the Early Token Request mechanism may, under certain circumstances, waste ring bandwidth (i.e., holding the Token while filling the FIFO). Therefore, it should be enabled only in those systems where the feature is specifically required.

If prestaging is enabled or a Service Opportunity exists for this Request Channel, data from the first ODU is loaded into the Request FIFO, and the MACSI device requests transmission from the Ring Engine. When the Ring Engine has captured the appropriate token and the frame is committed to transmission (the FIFO threshold has been reached or the end of the frame is in the FIFO), transmission begins. The MACSI device fetches the next ODUD and starts loading the ODUs of the next frame into the FIFO. This continues (across multiple service opportunities if required) until all frames for that Request have been transmitted (i.e., an REQ.ONLY or an REQ.LAST is detected) or an exception or error occurs which prematurely ends the Request.

The MACSI device will load REQ Descriptors as long as the RQSTOP bit in the State Attention Register is Zero, the REQ Queue contains valid entries (the REQ Queue Pointer Register does not exceed the REQ Queue Limit Register), and there is space in the CNF Queue (the MACSI device has not detected equality of the CNF Queue Pointer Register and the CNF Queue Limit Register).

Request status is generated as a single confirmation object (single- or multi-part) per Request object, with each confirmation object consisting of one or more CNF Descriptors. The type of confirmation is specified by the host in the Confirmation Class field of the REQ Descriptor.

The MACSI device can be programmed to generate CNF Descriptors at the end of the Request object (End Confirmation), or at the end of each token opportunity (Intermediate Confirmation), as selected in the E and I bits of the Confirmation Class Field of the REQ Descriptor. A CNF Descriptor is always written when an exception or error occurs (regardless of the value in the Confirmation Class field), when a Request is completed (for End or Intermediate Confirmation Class), or when a Service Opportunity ends (Intermediate Confirmation Class only).

There are three basic types of confirmation: Transmitter, Full, and None. With Transmitter Confirmation, the MACSI device verifies that the Output Data Units were successfully transmitted. With Full Confirmation, the Request Machine verifies that the ODUs were successfully transmitted, that the number of (returning) frames "matches" the number of transmitted ODUs, and that the returning frames contain the expected status. Full confirmation takes advantage of the fact that the sending station also removes its frames from the network. When the None Confirmation Class is selected, confirmation is written only if an exception or error occurs.

For Full Confirmation, a matching frame must meet the following criteria:

1. The frame has a valid Ending Delimiter (ED).
2. The selected bits in the FC fields of the transmitted and received frames are equal (the selected bits are specified in the FCT bit of the Request Configuration Register).
3. The frame is My__SA (MFLAG or both SAT & EM asserted).
4. The frame status indicators match the values in the Expected Frame Status Register.
5. FCS checking is disabled or FCS checking is enabled and the frame has a valid FCS.
6. All bytes from FC to ED have good parity (when the FLOW bit in the Mode Register is set, i.e., parity checking is enabled).

The confirmed frame count starts after the first Request burst frame has been committed by the Ring Engine, and when a frame with My__SA is received. Void and My__Void frames are ignored by the MACSI device. The frame count ends when any of the following conditions occur:

1. All frames have been transmitted, and the transmitted and confirmed frame counts are equal.
2. There is a MACRST (MAC Reset).
3. The state of the ring-operation has changed.
4. A stripped frame or a frame with a parity error is received.
5. A non-matching frame is received.
6. A token is received.

When Source Address Transparency is selected (by setting the SAT bit in the Request Configuration Register) and Full confirmation is enabled, confirmation begins when a frame end is detected with either MFLAG or EM asserted.

When a non-matching frame is received, the MACSI device ends the Request, and generates the Request Complete (RCM), Exception (EXC), and Breakpoint (BRK) attentions. Any remaining REQs in the Request object are fetched until a REQ.Last or REQ.Only is encountered. Processing then resumes on the next REQ.First or REQ.Only (any other type of REQ would be a consistency failure).

Request errors and exceptions are reported in the State Attention Register, Request Attention Register, and the Confirmation Message Descriptor. When an exception or error occurs, the Request Machine generates a CNF and ends the Request. The Unserviceable Request (USR) attention is set to block subsequent Requests once one becomes unserviceable.

6.2.3 State Machines

There are three state machines under control of the host: the Request Machine, the Indicate Machine, and the Status/Space Machine. Each Machine has two Modes: Stop and Run. The Mode is determined by the setting of the Machine's corresponding STOP bit in the State Attention Register. The STOP bits are set by the MACSI device when an error occurs or may be set by the user to place the state machine in Stop Mode.

The MACSI device Control Registers may be programmed only when all Machines are in Stop Mode. When the Status/Space Machine is in Stop Mode, only the Pointer RAM and Limit RAM Registers may be programmed. When the Indicate and Request Machines are in Stop Mode, all indicate and request operations are halted. When the Status/Space Machine is in Stop Mode, only the PTOP and LMOP service functions can be performed.

6.3 EXTERNAL MATCHING INTERFACE

This interface consists of four pins which are used to give the MACSI device additional address status about the incoming frame. ECIP is the timing signal. ECOPY and EM are used to report to the System Interface external matches of destination and source addresses respectively. EA and EM are used by the Ring Engine to control setting of the A indicator and frame stripping.

For the purposes of external matching, it is recommended that the frame data be viewed at the PLAYER+/MACSI Receive interface, (PID<7:0>, PIP, PIC). In addition it is recommended that the user design the circuit to detect the JK symbol at the MACSI/PLAYER+ interface to start address matching.

To instruct the MACSI device to copy a frame, the proper use of the ECIP, ECOPY, and EM pins is as follows. External address matching circuitry must assert ECIP some time from the arrival of the start delimiter (JK) to the 6th byte of the INFO field (as measured at the PLAYER+/MACSI interface). Otherwise, the MACSI device assumes that no external address comparison is taking place. ECIP must be negated for at least one cycle to complete the external comparison. If it has not been deasserted by the 2nd byte after the End Delimiter (ED), the frame is not copied. ECOPY and EM are sampled on the clock cycle after ECIP is negated. ECIP is ignored after it is negated until the arrival of the next JK.

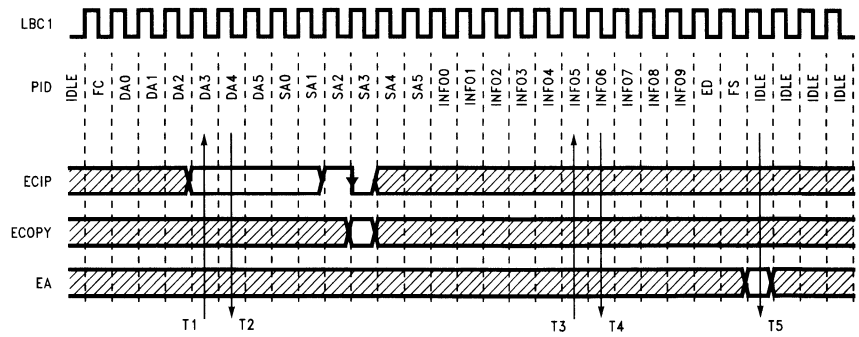


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FIGURE 6-2. MACSI Device External Matching Interface Timing

Note that this design allows ECIP to be a positive or negative pulse. To confirm frames in this mode, (typically with Source Address Transparency enabled), EM must be asserted within the same timeframe as ECOPY.

The Ring Engine samples EA two byte-times after the end delimiter (ED) is passed between the PLAYER+ device and the MACSI device. If EA is asserted, the MACSI device will transmit the A Indicator as an S. The Ring Engine samples EM continuously and will begin to strip a frame three byte-times after the assertion of EM. This implies that the user must ground EM if not used. The Ring Engine does not use the ECIP timing signal.

It is important to note that ECIP functions as an indicator to the internal MACSI device Indicate Machine to hold off the copying of incoming data until the ECIP line is negated. Therefore, even if a design does not intend to take advantage of the MACSI device External Address Matching interface, the user must still ensure that the ECIP signal line is properly negated. Also important is the fact that the MACSI device samples the ECIP signal line in order to detect just two conditions. It looks at whether ECIP is asserted at any time during the period between the start delimiter (JK) and the 6th byte of the INFO field and then waits until the deassertion of ECIP, at which point the MACSI device samples the ECOPY and EM signal lines for their status on this particular frame.

In the timing diagram (see *Figure 6-2*), the specific cycles shown for the assertion and deassertion of ECIP comprise only one possible valid timing. Other timings are valid as well, within the limits of the timing parameters to be described below. Shaded areas indicate cycles where the MACSI device is not sampling the signal lines for this particular pattern. Note that the sampling of ECIP is level sensitive and synchronous with LBC1.

Note that there are five timing parameters (T1–T5). T1 and T3 are limits as to when the initial assertion of ECIP will be recognized. Once ECIP is asserted, T2, T4, and T5 become timing limits on the deassertion of ECIP. Once deasserted, ECIP is not sampled further (until the start of the next frame).

T1 is the earliest cycle where the assertion of ECIP will be recognized. ECIP may be asserted earlier than this but the MACSI device will not sample it during these earlier periods. T1's timing is fixed as the fourth cycle following the FC data byte at the PLAYER+/MACSI interface.

T2 is the earliest cycle where the deassertion of ECIP will be recognized. This can occur as soon as one cycle following ECIP's assertion. ECIP needs to be asserted for a minimum of one full clock cycle.

T3 is the latest cycle where the initial assertion of ECIP will still be recognized. T3 must occur before the 6th byte of the INFO field, not afterward. If ECIP is asserted later than this cycle, an external match will not be recognized; i.e., the frame will be copied only if it is an internal match. When ECIP is not asserted until after T3, it is not recognized. This is the only case where maintaining ECIP's assertion during the frame will have no effect at all.

T4 is the latest cycle where the deassertion of ECIP will be recognized in "regular" fashion. That is, if ECIP is held asserted beyond T4, a special case is created within the MACSI device when the external compare has persisted to the point where it takes precedence over all other copy modes. In this case, all frames which are copied, regardless of whether it was an external match, internal match, or SMT frame, **are copied to ICHN2.** Note that even if an internal match has already occurred, ECIP must still become deasserted for the frame copy to complete.

It is important to note that the timing shown for T4 is dependent on the setting of the SMLB bit of the MACSI device's Mode Register 0 (MR0). The timing shown in *Figure 6-2* is for frame copies in small-burst mode only. T4 signifies the boundary condition internal to the MACSI device where the first full burst of data has been received. The ABus write access for this data will then automatically default to ICHN2 if an external copy decision is still pending, **regardless of sort mode.** When the SMLB bit is not set, i.e., in large burst mode, T4 would occur 16 cycles later than shown in *Figure 6-2.*

T5 is the final cycle where the deassertion of ECIP can be recognized, and it occurs two cycles after the end delimiter (ED) is transferred between the PLAYER+ and MACSI devices. If ECIP is held high beyond this point, the frame will not be copied at all, **even if an internal match occurred.** Note that this is true even if Internal/External sorting is not

enabled. Therefore, for applications which do not use external address matching, ECIP should be tied low. Note also that if ECIP remains asserted to the point where the incoming frame data completely fills the MACSI device's Indicate Data FIFO (4608 bytes for a MACSI device), then the frame will be dropped due to a FIFO overrun.

6.4 BUS INTERFACE UNIT

6.4.1 Overview

The ABus provides a 32-bit wide synchronous multiplexed address/data bus for transfers between the host system and the MACSI device. The ABus uses a bus request/bus grant protocol that allows multiple bus masters, supports burst transfers of 16 and 32 bytes, and supports virtual and physical addressing using fixed-size pages. The MACSI device is capable of operating directly on the system bus to main memory or connected to external shared memory.

All bus signals are synchronized to the master bus clock. The maximum burst speed is one 32-bit word per clock, but slower speeds may be accommodated by inserting wait states. The user may use separate clocks for the ring (FDDI MAC) and system (ABus) interfaces. The only restriction is that the ABus clock must be at least as fast as the ring clock (LBC). It is important to note that all ABus outputs change and all ABus inputs are sampled on the rising edge of AB_CLK.

The MACSI device has two major modes of ABus operation. The default, or "normal" mode, corresponds to the original BSI device and is completely backward compatible. The second mode is the Enhanced ABus mode. This mode is intended to reduce the logic required to interface to the SBus originally developed by Sun Microsystems, Inc. When the enhanced mode is selected, the MACSI device timing and interface signals are modified slightly to create a closer fit to the SBus. This lowers the cost and eases design of SBus FDDI adapter cards. This new mode is accessible by programming a mode bit in a register (MR1.EAM = 1). This bit is set to an inactive state upon reset to maintain backward compatibility with the original BSI device.

Addressing Modes

In the default ABus mode, The Bus Interface Unit has two Address Modes, as selected by the user: Physical Address Mode and Virtual Address Mode. In Physical Address Mode, the MACSI device emits the memory address and immediately begins transferring the data. In Virtual Address Mode, the MACSI device inserts two clock cycles and TRI-STATE® the address between emitting the virtual address and starting to transfer the data. This allows virtual-to-physical address translation by an external memory mapping unit (MMU).

The MACSI device has a mode for controlling the ABus Address Strobe ($\overline{AB\_AS}$). In the default mode, $\overline{AB\_AS}$ is driven active during the address cycle and remains low throughout the access. In the second mode (MR1.ASM = 1), $\overline{AB\_AS}$ is driven active during the address cycle and driven inactive during the remainder of the access. This allows $\overline{AB\_AS}$ to be used directly as a clock enable to the address latching device which reduces the number of external components.

In Enhanced ABus Mode (EAM), the MACSI device has fixed address timing which is similar to the Physical address timing described above. The SBus MMU does not require extra cycles for the address translation.

The MACSI device interfaces to byte-addressable memory, but always transfers information in words. The MACSI device uses a word width of 32 data bits plus 4 (1 per byte) parity bits. Parity may be ignored.

Bus Transfers

The ABus supports single word accesses and 4-word and 8-word bursts. Simple reads and writes involve a single address and data transfer. Burst reads and writes involve a single address transfer followed by multiple data transfers. Burst sizes are selected dynamically by the MACSI device. The user can disable 8-word bursts by setting MR0.SMLB to a 1. This forces the MACSI device to use 1-word and 4-word transactions only.

The MACSI device provides the full de-multiplexed address during an access. This includes the word address for each word of a burst (AB_A[4:2]). In order to use the de-multiplexed addresses AB_A[27:5], the Address Timing Mode bit (MR1.ATM) must be set equal to one. This causes the word address to come out in the same cycle as the word of data being accessed. The word addresses signals (AB_A[4:2]) may be used in the "lookahead" mode (MR1.ATM = 0) if the user does address de-multiplexing externally by latching AB_A[27:5] externally during the address cycle.

On Indicate Channels, when 8-word bursts are enabled, all transactions will be 8 words until the end of the frame; the last transfer will be 4 or 8 words, depending on the number of remaining bytes. If only 4-word bursts are allowed, all Indicate Data transfers are 4 words.

On Request Channels, the MACSI device will use 4- or 8-word bursts to access all data up to the end of the ODU. If 8-word bursts are enabled, the first access will be an 8-word burst if the ODU begins less than 4 words from the start of an 8-word burst boundary. If 8-word bursts are not allowed, or if the ODU begins 4 or more words from the start of an 8-word burst boundary, a 4-word burst will be used. The MACSI device will ignore unused bytes if the ODU does not start on a burst boundary. At the end of an ODU, the MACSI device will use the smallest transfer size (1, 4, or 8 words) which completes the ODU read. To coexist in a system that assumes implicit wrap-around for the addresses within a burst, the MACSI device never emits a burst that will wrap the 4- or 8-word boundary.

A Function Code identifying the type of transaction is output by the MACSI device on the upper four address bits during the address phase of a data transfer. This can be used for more elaborate external addressing schemes such as directing control information to one memory and data to another (e.g., an external FIFO).

Byte Ordering

The basic addressable unit is a byte so request data may be aligned to any byte boundary in memory. All information is accessed in 32-bit words, however, so the MACSI device ignores unused bytes when reading.

Descriptors must always be aligned to a 32-bit word address boundary. Input Data Units are always aligned to a burst-size boundary. Output Data Units may be any number of bytes, aligned to any byte-address boundary but operate most efficiently when aligned to a burst-size boundary. Pool Space Descriptors (PSPs) **must** point to a burst boundary or the Receive data will not be written to memory correctly.

Burst transfers are always word-aligned on a 16- or 32-byte (burst-size) address boundary. Burst transfers will never cross a burst-size boundary. If a 32-byte transfer size is enabled (MR0.SMLB = 0), the MACSI device will perform both 16-byte and 32-byte bursts, whichever is most efficient (least number of clocks to load/store all required data). If the MACSI device has less than a full burst of data to complete a frame, it will write a full burst. Random data is written to the unused locations. The host uses the IDUD length field to determine where the valid data bytes end.

The Bus Interface Unit can operate in either Big Endian or Little Endian Mode. The bit and byte alignments for both modes are shown in *Figure 6-3.* Byte 0 is the first byte received from the ring or transmitted to the ring. This mode affects the placement of frame data bytes but it does not affect the order of Descriptor bytes.

Big-Endian Byte Order

D[31]			D[0]
Word			
Halfword 0		Halfword 1	
Byte 0	Byte 1	Byte 2	Byte 3

Little-Endian Byte Order

D[31]			D[0]
Word			
Halfword 1		Halfword 0	
Byte 3	Byte 2	Byte 1	Byte 0

FIGURE 6-3. ABus Byte Orders

Bus Arbitration

The ABus is a multi-master bus, using a simple Bus Request/Bus Grant protocol that allows an external Bus Arbiter to support any number of bus masters, using any arbitration scheme (e.g., rotating or fixed priority). The protocol provides for multiple transactions per tenure and bus master preemption.

The MACSI device asserts a Bus Request, and assumes mastership when Bus Grant is asserted. If the MACSI device has another transaction pending, it will keep Bus Request asserted, or reassert it before the completion of the current transaction. Note that Bus Request is guaranteed to be de-asserted for at least two cycles when MR1.EAM is enabled. It is a requirement of the SBus specification that Bus Request be de-asserted between each transaction. If Bus Grant is (re)asserted before the end of the current transaction, the MACSI device retains mastership and runs the next transaction. This process may be repeated indefinitely.

It is important to note that in default ABus mode (MR1.EAM = 0), the MACSI device may take up to two cycles to detect the assertion of Bus Grant. Therefore, the external interface logic must not remove Bus Grant or latch addresses until a signal such as Address Strobe is asserted indicating that the MACSI device has recognized the Bus Grant.

If the Bus Arbiter wishes to preempt the MACSI device, it deasserts Bus Grant. The MACSI device will complete the current bus transaction, then release the bus. From preemption to bus release is a maximum of (11 bus clocks + (8 times the number of memory wait states)) bus clocks. For example, in a 1 wait-state system, the MACSI device will release the bus within a maximum of 19 bus clocks.

Parity

The state of the FLOW bit in Mode Register 0 (MR0.FLOW) controls two MACSI device modes: one for systems using parity, the other for systems not using parity.

Regardless of the state of MR0.FLOW, the MACSI device always provides odd parity on ABus address cycles, and Control Bus read cycles. Parity is never checked by the MACSI device on ABus read cycles. The ABus data parity, (except for Descriptor data parity which is generated internally) flows directly from the Ring Engine interface. If parity checking is enabled within the Ring Engine, parity flows up from the PLAYER+ interface. If parity checking is disabled within the Ring Engine, good parity is generated at the Ring Engine/Service Engine interface.

For transmit frame data, the parity from the ABus flows directly to the Ring Engine interface when MR0.FLOW is asserted. The data integrity across the ABus and through the Service Engine may be checked by enabling parity checking within the Ring Engine. If the MR0.FLOW bit is deasserted, the MACSI device will generate good parity at the transmit data (MR7–0) Ring Engine interface.

When MR0.FLOW is enabled, parity is checked on Control Bus write operations. If a parity error is detected, the write access is rejected and the STAR.CPE bit is asserted. When MR0.FLOW is disabled Control Bus write parity is ignored.

When MR0.FLOW is enabled, parity is checked on MAC Indicate interface (receive data from the Ring Engine). If an error is detected, the STAR.BPE will be asserted and the IDUD for that frame will carry a status of "parity error". When MR0.FLOW is disabled, the parity bit at the MAC Indicate interface is ignored.

Bandwidth

The ABus supports single reads and writes, and burst reads and writes. With physical addressing, back-to-back single reads/writes can take place every four clock cycles. Burst transactions can transfer 8, 32-bit words (32 bytes) every 11 clock cycles. With a 25 MHz clock this yields a peak bandwidth of 72.7 Mbytes/sec.

To allow the bus to operate at high frequency, the protocol defines all signals to be both asserted and deasserted by the bus master and slaves. Having a bus device actively deassert a signal guarantees a high-speed inactive transition. If this were not defined, external pull-up resistors would not be able to deassert signals fast enough. The protocol also reduces contention by avoiding cases where two bus devices simultaneously drive the same line.

6.0 Functional Description (Service Engine) (Continued)

The MACSI device operates synchronously with the ABus clock. In general, operations will be asynchronous to the ring, since most applications will use a system bus clock that is asynchronous to the ring. The MACSI device is designed to interface either directly to the host's main system bus or to external shared memory. When interfaced to the host's bus, there are two parameters of critical interest: latency and bandwidth.

Data moves between the Request and Indicate Channels and the ABus via four FIFOs, two in the receive path (Indicate) and two in the transmit path (Request). There are two, 1152 x 36-bit data FIFOs for Indicate and Request data (4608 byte of data FIFO in each direction). On the ABus Interface, there are two Burst FIFOs, each containing two banks of 32 bytes which provide ABus bursting capability.

The amount of latency covered by the Data FIFO plus one of the banks of the Burst FIFO must meet the average and maximum bus latencies of the external memory. With a new byte every 80 ns from the ring, a 4608 byte FIFO provides 4608×80 ns $= 368.64$ μs maximum latency. The two 32 byte burst FIFO in each direction provide an additional 5.1 μs of latency.

To assist latency issues, the MACSI device can completely empty or fill the Burst FIFO in one bus tenure by asserting Bus Request for multiple transactions. Since one bank of the Burst FIFO is 8 words deep, if 8-word bursts are enabled, that half of the Burst FIFO can be emptied in one transaction. If the second half of the burst FIFO is also full, it can be emptied in the same bus tenure by again granting the bus to the MACSI device.

The MACSI device may be preempted at any time by removing Bus Grant, causing the MACSI device to complete the current transaction and release the bus. There will be a maximum of 11 clocks (plus any memory wait states) from preemption to bus release (fewer if 8-word bursts are not enabled).

6.4.2 Bus States

An ABus Master has eight states: idle (Ti), bus request (Tbr), virtual address (Tva), MMU translate (Tmmu), physical address (Tpa), data transfer (Td), wait (Tw) and recovery (Tr).

An ABus Slave has five states: idle (Ti), selected (Ts), data transfer (Td), wait (Tw), and recovery (Tr).

Master States

The Ti state exists when no bus activity is required. The BIU does not drive any of the bus signals when it is in this state (all are released). If the BIU requires bus service, it may assert Bus Request.

When a transaction occurs, the BIU enters Tbr, asserts Bus Request, and then waits for Bus Grant to be asserted.

The state following Tbr is either Tva or Tpa. In Virtual Address Mode, the BIU enters Tva and drives the virtual address and size lines onto the bus. In Physical Address Mode, Tpa occurs next (see Section 6.4.3).

Following a Tva state is a Tmmu state. During this cycle the external MMU is performing a translation of the virtual address emitted during Tva.

Following a Tmmu state (when using virtual addressing) or a Tbr state (when using physical addressing), is the Tpa state. During the Tpa state, the MACSI device drives the read/write strobes and size signals. In physical address mode, it also drives AB__AD with address. In virtual address mode, the MACSI device TRI-STATEs AB__BD so the host CPU or MMU can drive the address.

Following the Tpa state, the BIU enters the Td state to transfer data words. Each data transfer may be extended indefinitely by inserting Tw states. A slave acknowledges by asserting $\overline{\text{AB\_\_ACK}}$ and transferring data in a Td state (cycle). If the slave can drive data at the rate of one word per clock (in a burst), it keeps $\overline{\text{AB\_\_ACK}}$ asserted.

Following the final Td/Tw state, the BIU enters a Tr state to allow time to turn off or turn around bus transceivers.

A bus retry request is recognized in any Td/Tw state. The BIU will go to a Tr state and then rerun the transaction when it obtains a new Bus Grant. The whole transaction is retried, i.e., all words of a burst. Additionally, no other transaction will be attempted before the interrupted one is retried. The BIU retries indefinitely until either the transaction completes successfully, or a bus error is signaled.

Bus errors are recognized in Td/Tw states.

6.0 Functional Description (Service Engine) (Continued)

6.4.3 Physical Addressing Bus Transactions

Bus transactions in Physical Address Mode are shown in *Figure 6-4* through *Figure 6-7*. MACSI device signals are defined in Section 8.

Single Read

Tbr: MACSI device asserts $\overline{AB\_BR}$ to indicate it wishes to perform a transfer. Host asserts $\overline{AB\_BG}$. The MACSI device moves to Tpa within the next three clocks.

Tpa: MACSI device drives AB_A and AB_AD with the address, asserts $\overline{AB\_AS}$, drives AB_$R/\overline{W}$ and AB_SIZ[2:0], and negates $\overline{AB\_BR}$ if another transaction is not required.

Td: MACSI device negates $\overline{AB\_AS}$, asserts $\overline{AB\_DEN}$, and samples $\overline{AB\_ACK}$ and $\overline{AB\_ERR}$. Slave asserts $\overline{AB\_ACK}$, drives $\overline{AB\_ERR}$, drives AB_AD (with data) when ready. The MACSI device samples a valid $\overline{AB\_ACK}$, capturing the read data. Tw states may occur after Td.

Tr: MACSI device negates AB_$R/\overline{W}$, $\overline{AB\_DEN}$, and AB_SIZ[2:0], and releases AB_A and $\overline{AB\_AS}$. Slave deasserts $\overline{AB\_ACK}$ and $\overline{AB\_ERR}$, and releases AB_AD.

Single Write

Tbr: MACSI device asserts $\overline{AB\_BR}$ to indicate it wishes to perform a transfer. Host asserts $\overline{AB\_BG}$. The MACSI device moves to Tpa within the next three clocks.

Tpa: MACSI device drives AB_A and AB_AD with the address, asserts $\overline{AB\_AS}$, drives AB_$R/\overline{W}$ and AB_SIZ[2:0], and negates $\overline{AB\_BR}$ if another transaction is not required.

Td: MACSI device negates $\overline{AB\_AS}$, asserts $\overline{AB\_DEN}$, drives AB_AD with the write data and starts sampling $\overline{AB\_ACK}$ and $\overline{AB\_ERR}$. Slave captures AB_AD data, asserts $\overline{AB\_ACK}$, and drives $\overline{AB\_ERR}$. Tw states may occur after Td if the slave deasserts $\overline{AB\_ACK}$.

Tr: MACSI device negates AB_$R/\overline{W}$, $\overline{AB\_DEN}$, and AB_SIZ[2:0], and releases AB_A, AB_AD, and $\overline{AB\_AS}$. Slave deasserts $\overline{AB\_ACK}$ and $\overline{AB\_ERR}$ and stops driving AB_AD with data.

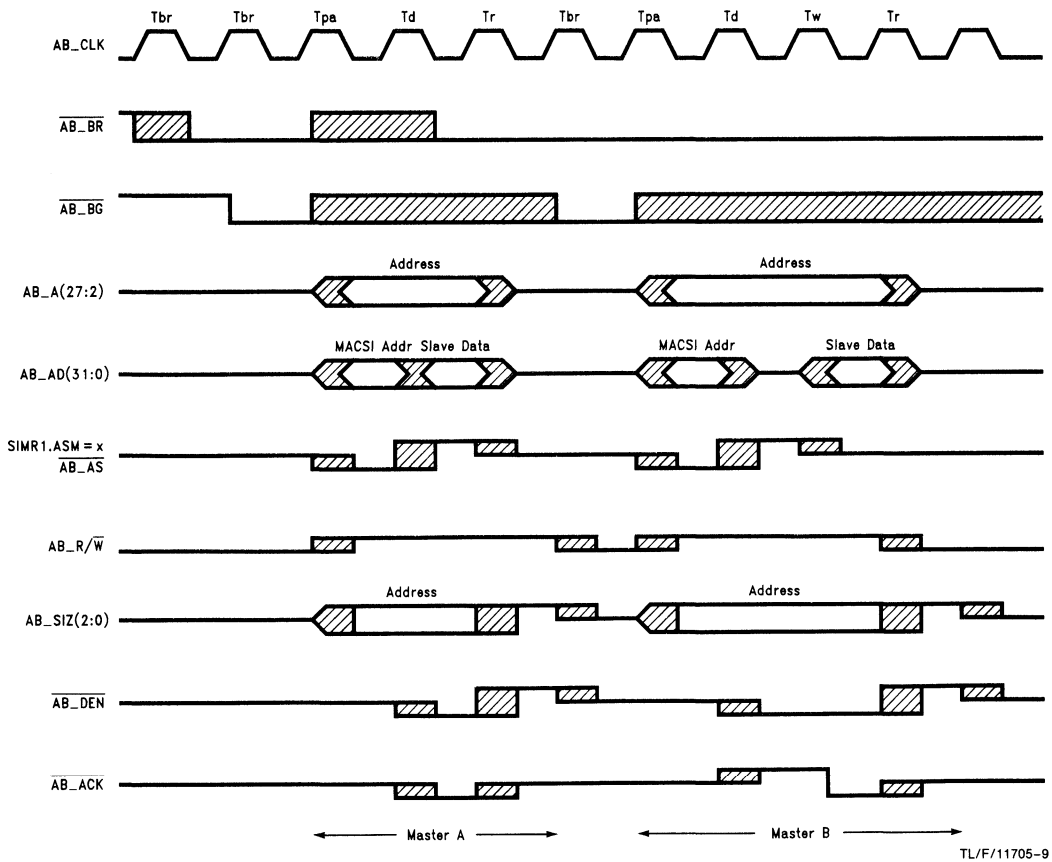

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FIGURE 6-4. ABus Single Read: Physical Addressing—0 w/s, 1 w/s

6.0 Functional Description (Service Engine) (Continued)

Burst Read

Tbr: MACSI device asserts AB__BR to indicate it wishes to perform a transfer. Host asserts AB__BG. The MACSI device moves to Tpa within the next three clocks.

Tpa: MACSI device drives AB__A and AB__AD with the address, asserts AB__AS, drives AB__R/W and AB__SIZ[2:0], and negates AB__BR if another transaction is not required.

Td: MACSI device asserts AB__DEN, samples AB__ACK and AB__ERR, and increments the address on AB__A. Slave asserts AB__ACK, drives AB__ERR, and drives AB__AD (with data) when ready. MACSI device samples a valid AB__ACK to capture the read data. Tw states may occur after Td. Td state is repeated four or eight times (according to the burst size). If MR1.ASM = 0, the MACSI device negates AB__AS in the last Td cycle. If MR1.ASM = 1, the MACSI device will negate AB__AS in the first Td cycle.

Tr: MACSI device negates AB__R/W, AB__DEN, and AB__SIZ[2:0], and releases AB__A and AB__AS. Slave deasserts AB__ACK and AB__ERR and releases AB__AD.

Burst Write

Tbr: MACSI device asserts AB__BR to indicate it wishes to perform a transfer. Host asserts AB__BG. The MACSI device moves to Tpa within the next three clocks.

Tpa: MACSI device drives AB__A and AB__AD with the address, asserts AB__AS, drives AB__R/W and AB__SIZ[2:0], and negates AB__BR if another transaction is not required.

Td: MACSI device asserts AB__DEN, drives AB__AD with the write data, samples AB__ACK and AB__ERR, and increments the address on AB__A. Slave captures AB__AD data, asserts AB__ACK, drives AB__ERR. MACSI device samples a valid AB__ACK. Tw states may occur after Td. Td state is repeated as required for the complete burst. If MR1.ASM = 0, the MACSI device negates AB__AS in the last Td cycle. If MR1.ASM = 1, the MACSI device will negate AB__AS in the first Td cycle.

Tr: MACSI device negates AB__R/W, AB__DEN, and AB__SIZ[2:0], releases AB__A and AB__AS, and stops driving AB__AD with data. Slave deasserts AB__ACK and AB__ERR.

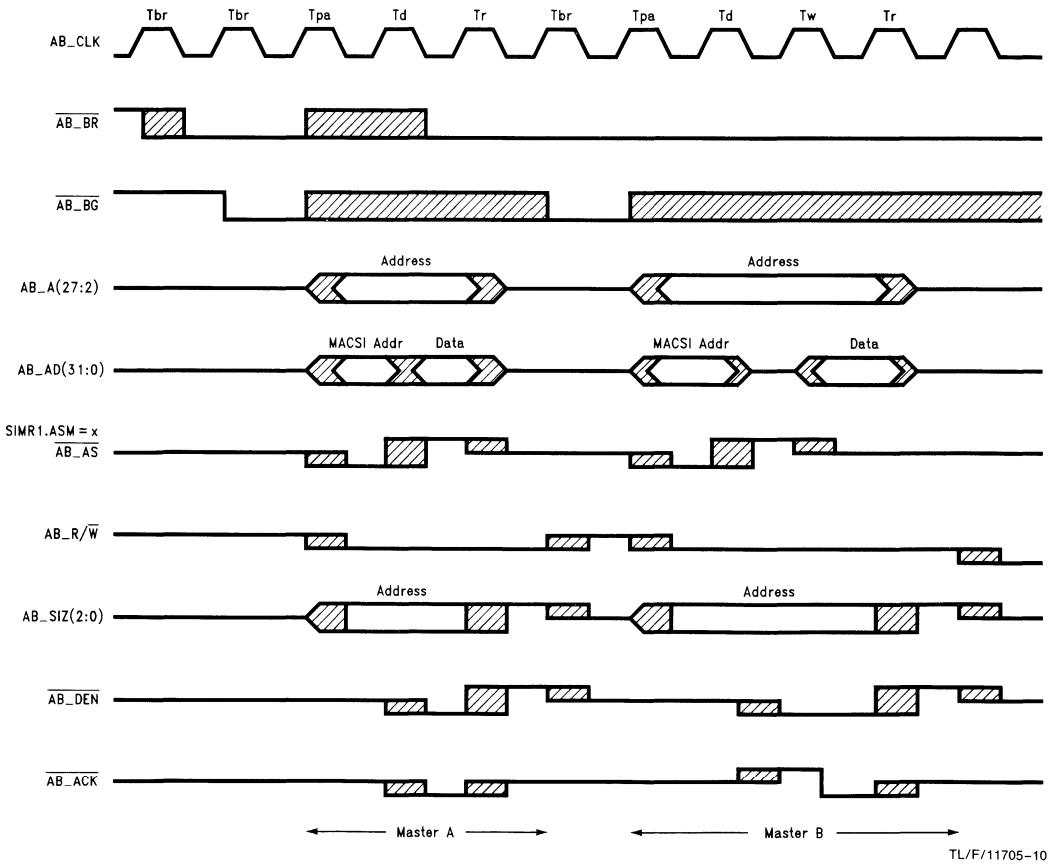

FIGURE 6-5. ABus Single Write: Physical Addressing—0 w/s, 1 w/s

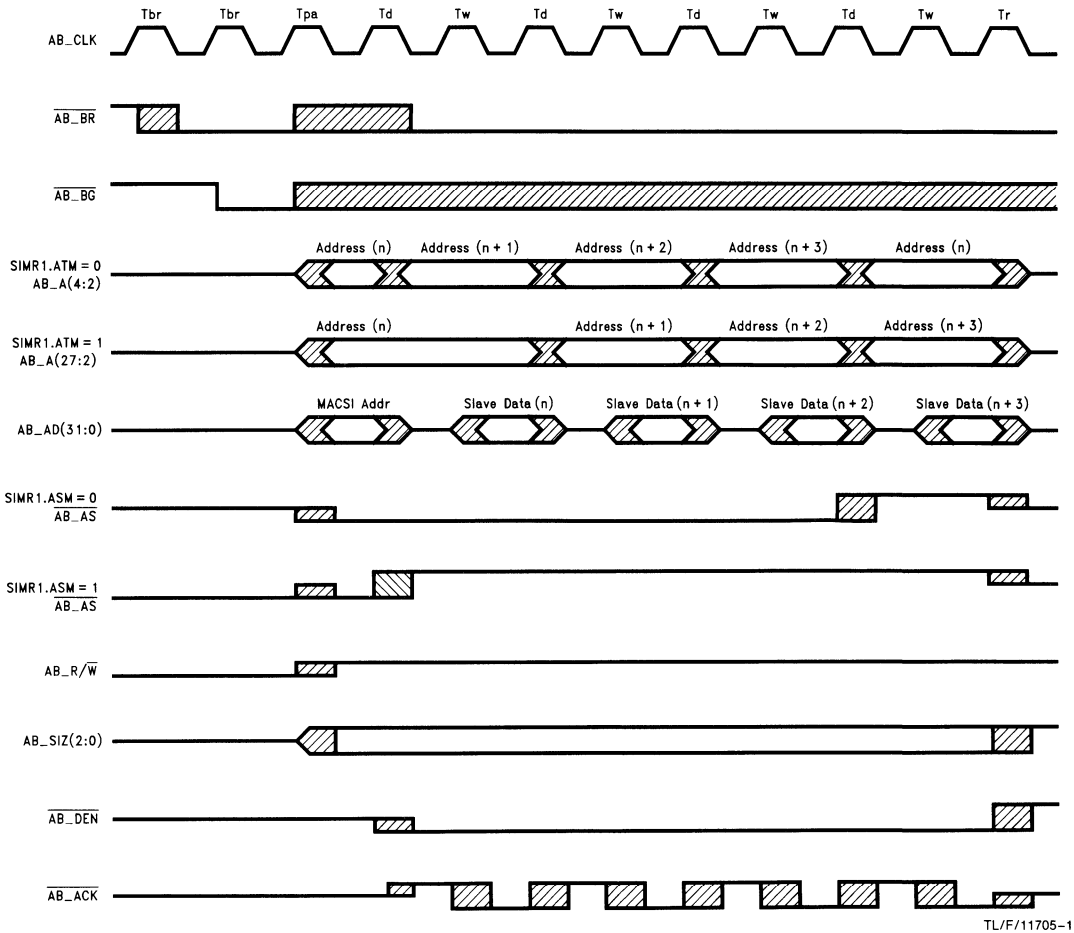

FIGURE 6-6. ABus Burst Read: Physical Addressing—16 Bytes, 1 w/s

6.4.4 Virtual Addressing Bus Transactions

Single Read

Tbr: MACSI device asserts AB__BR to indicate it wishes to perform a transfer. Host asserts AB__BG. The MACSI device moves to Tva within the next three clocks, and then drives AB__A and AB__AD.

Tva: MACSI device drives AB__A and AB__AD with the virtual address for one clock, negates AB__AS, asserts AB__R/W, drives AB__SIZ[2:0], and negates AB__BR if another transaction is not required.

Tmmu: Host MMU performs an address translation during this clock.

Tpa: Host MMU drives AB__AD with the translated (physical) address.

Td: MACSI device negates AB__AS, asserts AB__DEN, and samples AB__ACK and AB__ERR. Slave asserts AB__ACK, drives AB__ERR, and drives AB__AD (with data) when ready. MACSI device samples a valid AB__ACK, and captures the read data. Tw states may occur after Td.

Tr: MACSI device negates AB__R/W, AB__DEN, and AB__SIZ[2:0], and releases AB__A and AB__AS. Slave deasserts AB__ACK and AB__ERR and releases AB__AD.

Single Write

Tbr: MACSI device asserts AB__BR to indicate it wishes to perform a transfer. Host asserts AB__BG. The MACSI device moves to Tva within the next three clocks, and then drives AB__A and AB__AD.

Tva: MACSI device drives AB__A and AB__AD with the virtual address for one clock, negates AB__AS, negates AB__R/W, and drives AB__SIZ[2:0].

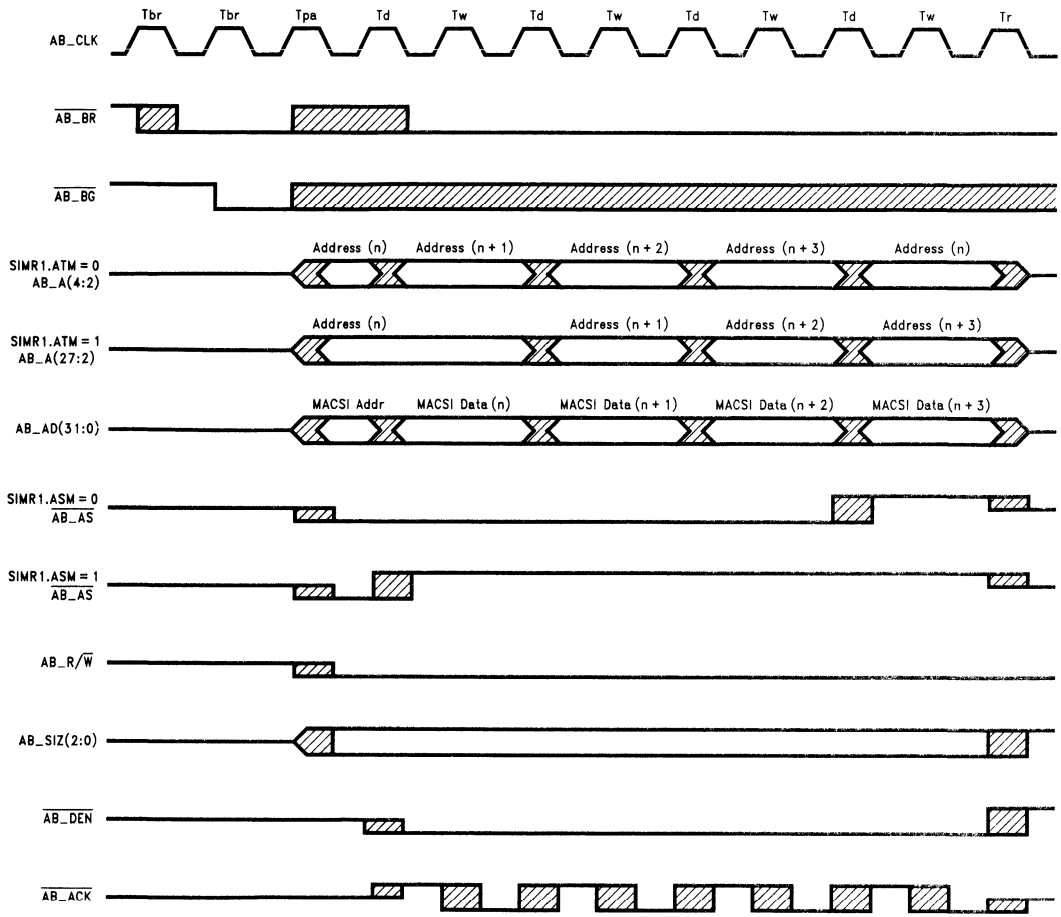

FIGURE 6-7. ABus Burst Write: Physical Addressing—16 Bytes, 1 w/s

Tmmu: Host MMU performs an address translation during this clock.

Tpa: Host MMU drives AB__AD with the address.

Td: MACSI device negates AB__AS, asserts AB__DEN, drives AB__AD with the write data and starts sampling AB__ACK and AB__ERR. Slave captures AB__AD data, asserts AB__ACK, and drives AB__ERR. MACSI device samples a valid AB__ACK. Tw states may occur after Td.

Tr: MACSI device negates AB__R/W, AB__DEN, and AB__SIZ[2:0], and releases AB__A, AB__AD, and AB__AS. Slave deasserts AB__ACK and AB__ERR and stops driving AB__AD with data.

Burst Read

Tbr: MACSI device asserts AB__BR to indicate it wishes to perform a transfer. Host asserts AB__BG. The MACSI device moves to Tva within the next three clocks, and then drives AB__A and AB__AD.

Tva: MACSI device drives AB__A and AB__AD with the virtual address for one clock, negates AB__AS, asserts AB__R/W, drives AB__SIZ[2:0], and negates AB__BR if another transaction is not required.

Tmmu: Host MMU performs an address translation during this clock.

Tpa: Host MMU drives AB__AD with the translated (physical) address.

Td: MACSI device asserts AB_DEN and samples AB_ACK and AB_ERR. Slave asserts AB_ACK, drives AB_ERR, and drives AB_AD (with data) when ready. MACSI device samples a valid AB_ACK, and captures the read data. Tw states may occur after Td. This state is repeated four or eight times (according to burst size). If MR1.ASM = 0 the MACSI device negates AB_AS in the last Td cycle. If MR1.ASM = 1, the MACSI device will negate AB_AS in the first Td cycle.

Tr: MACSI device negates AB_R/W, AB_DEN, and AB_SIZ[2:0], and releases AB_A and AB_AS. Slave deasserts AB_ACK and AB_ERR and releases AB_AD.

Burst Write

Tbr: MACSI device asserts AB_BR to indicate it wishes to perform a transfer. Host asserts AB_BG. The MACSI device moves to Tva within the next three clocks, and then drives AB_A and AB_AD.

Tva: MACSI device drives AB_A and AB_AD with the virtual address for one clock, negates AB_AS, negates AB_R/W, drives AB_SIZ[2:0].

Tmmu: Host MMU performs an address translation during this clock.

Tpa: Host MMU drives AB_AD with the address.

Td: MACSI device asserts AB_DEN, drives AB_AD with the write data, and starts sampling AB_ACK and AB_ERR. Slave captures AB_AD data, asserts AB_ACK and drives AB_ERR. MACSI device samples a valid AB_ACK. Tw states may occur after Td. Td is repeated as required for the complete burst. If MR1.ASM = 0, the MACSI device negates AB_AS in the last Td cycle. If MR1.ASM = 1, the MACSI device will negate AB_AS in the first Td cycle.

Tr: MACSI device negates AB_R/W, AB_DEN, and AB_SIZ[2:0], releases AB_A, AB_AD, and AB_AS, and stops driving AB_AD with data. Slave deasserts AB_ACK and AB_ERR.

6.5 ENHANCED ABUS MODE

When the enhanced ABus mode is selected, several changes occur. The timing of AB_ACK is modified during read accesses. In this mode, read data is expected one cycle after the AB_ACK signal (see *Figure 6-8* and *Figure 6-11*). In addition, channel information is no longer supplied on the upper four bits of the Address/Data lines during the address cycle. Instead, the value of this nibble of address is supplied from a programmable register within the MACSI device (for a full description of these bits please see System Interface Mode Register1 (SIMR1)). Finally, the AB_DEN signal becomes an input in this enhanced mode. This signal, along with AB_ACK and AB_ERR, are used to encode a subset of the acknowledge, retry, and error functions supported on the SBus.

These enhancements make it easier to connect the MACSI device to the SBus as a bus master. However, a full FDDI adapter design requires the design of a slave interface from the SBus to the control bus of the MACSI device and the other FDDI components.

6.5.1 Enhanced ABus Mode Bus Transactions

Bus transactions in the Enhanced Abus Mode are shown in *Figure 6-8* through *Figure 6-11*. In the Enhanced ABus mode, the Bus Request signal (AB_BR) will be deasserted after the bus is granted until the completion of the bus transaction. The only exception to this may occur when the MACSI device is attempting back-to-back burst reads. In this case AB_BR may be deasserted for as few as two cycles.

Single Read

Tbr: MACSI device asserts AB_BR to indicate it wishes to perform a transfer. Host asserts AB_BG. The MACSI device moves to Tma on the next cycle.

Tma: MACSI device drives AB_A and AB_AD with the master address, asserts AB_AS, drives AB_R/W and AB_SIZ[2:0], and negates AB_BR until the end of this transaction.

Tpa: The Physical address is asserted by the MMU.

Td: MACSI device negates AB_AS and samples AB_ACK, AB_ERR, and AB_DEN. Slave asserts AB_ACK, AB_ERR, and AB_DEN with the appropriate acknowledgment. The MACSI device samples a valid acknowledgment and moves to Tr. Tw states may occur after Td.

Tr: MACSI device negates AB_R/W, AB_DEN, and AB_SIZ[2:0], releases AB_A and AB_AS, and samples AB_AD. Slave drives AB_AD (with data), deasserts AB_ACK, AB_ERR, and AB_DEN, and releases AB_AD.

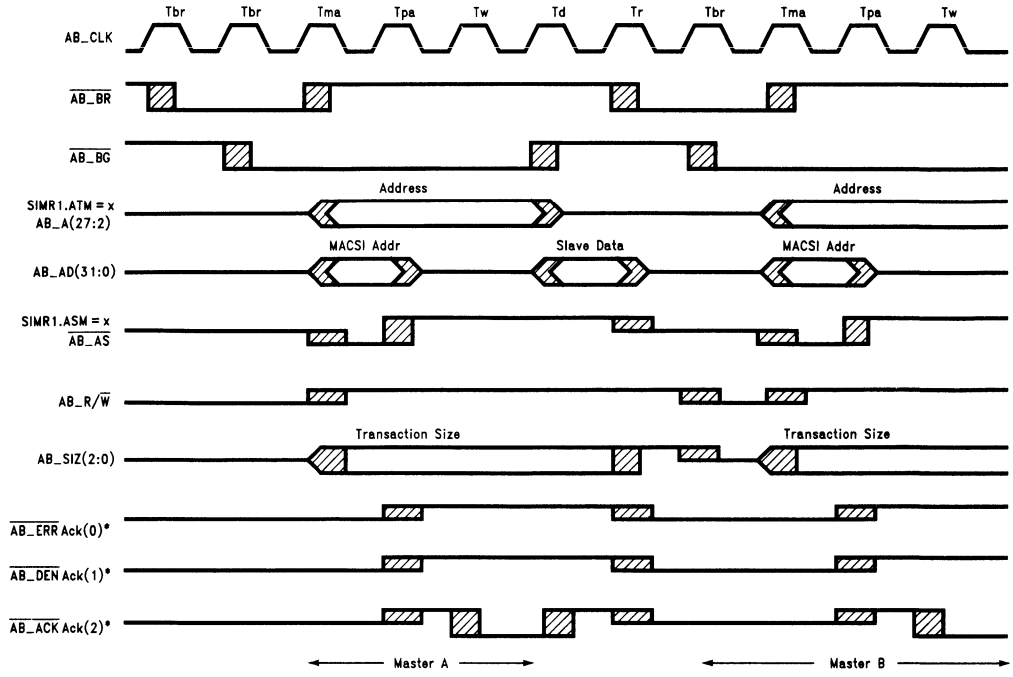

FIGURE 6-8. Enhanced ABus Read Timing—0 w/s, 1 w/s

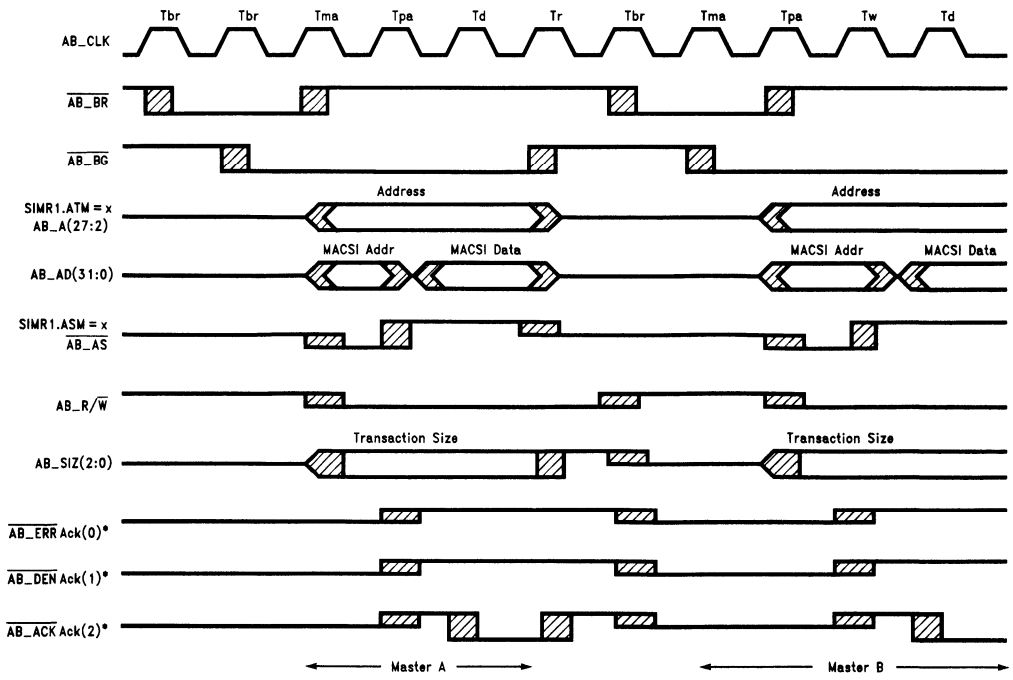

FIGURE 6-9. Enhanced ABus Mode Write Timing

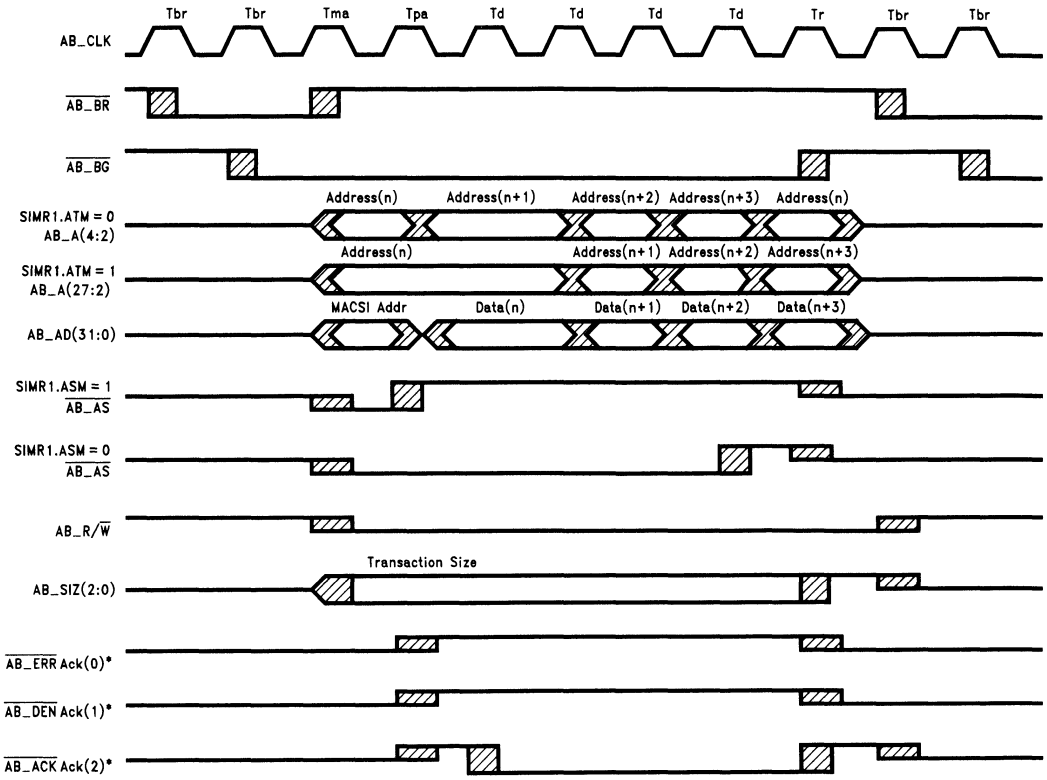

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FIGURE 6-10. Enhanced ABus Mode Burst Write Timing

Single Write

Tbr: MACSI device asserts AB_BR to indicate it wishes to perform a transfer. Host asserts AB_BG. The MACSI device moves to Tma in the next cycle.

Tma: MACSI device drives AB_A and AB_AD with the master address, asserts AB_AS, drives AB_R/W and AB_SIZ[2:0], and negates AB_BR until the end of this transaction.

Tpa: The Physical address is asserted by the MMU.

Td: MACSI device negates AB_AS, drives AB_AD with the write data and starts sampling AB_ACK, AB_ERR, and AB_DEN. Slave captures AB_AD data, and acknowledges with AB_ACK, AB_ERR, and AB_DEN. Tw states may occur after Td if the slave does not acknowledge.

Tr: MACSI device negates AB_R/W, AB_SIZ[2:0], releases AB_A, AB_AD, and AB_AS, and stops driving AB_AD with data. Slave deasserts AB_ACK, AB_ERR, and AB_DEN.

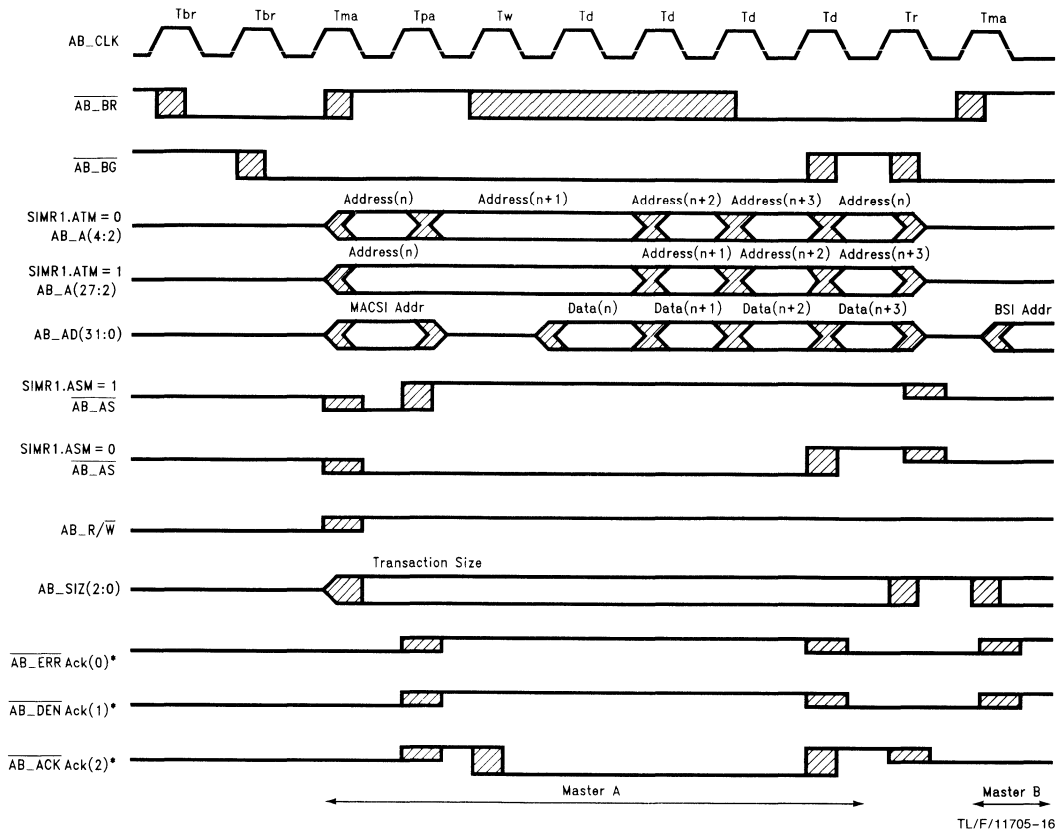

FIGURE 6-11. Enhanced ABus Mode Back-to-Back Read Timing

Burst Read

Tbr: MACSI device asserts AB_BR to indicate it wishes to perform a transfer. Host asserts AB_BG. The MACSI device moves to Tma in the next cycle. This cycle may be skipped if AB_BR was asserted during the previous access. This allows for back-to-back burst reads.

Tma: MACSI device drives AB_A and AB_AD with the master address, asserts AB_AS, drives AB_R/W and AB_SIZ[2:0], and negates AB_BR for at least two cycles.

Tpa: The Physical Address is asserted by the MMU.

Td: MACSI device samples AB_ACK, AB_ERR, and AB_DEN, and increments the address on AB_A. Slave acknowledges using AB_ACK, AB_ERR, and AD_DEN. MACSI device samples a valid AB_ACK and latches data in the **following** cycle. Tw states may occur after Td. Td state is repeated four or eight times (according to the burst size). If MR1.ASM = 0, the MACSI device negates AB_AS in the last Td cycle. If MR1.ASM = 1, the MACSI device negates AB_AS in the first Td cycle.

Tr: MACSI device negates AB_R/W and AB_SIZ[2:0] and releases AB_A and AB_AS. Slave drives AB_AD (with data), deasserts AB_ACK, AB_ERR, and AB_DEN. If another request is pending (AB_BR asserted) and the Bus is regranted in this cycle, the MACSI device will proceed directly to the Tma state of the next burst. The normal Tbr state is skipped allowing back-to-back burst reads.

Burst Write

Tbr: MACSI device asserts AB_BR to indicate it wishes to perform a transfer. Host asserts AB_BG. The MACSI device moves to Tma in the next cycle.

Tma: MACSI device drives AB_A and AB_AD with the master address, asserts AB_AS, drives AB_R/W and AB_SIZ[2:0], and negates AB_BR until this transaction is completed.

Tpa: The Physical Address is asserted by the MMU.

Td: MACSI device drives AB_AD with the write data, samples AB_ACK, AB_ERR, and AB_DEN, and increments the address on AB_A. Slave captures AB_AD data and acknowledges using AB_ACK, AB_ERR, and AB_DEN. MACSI device samples a valid acknowledge. Tw states may occur after Td. Td state is repeated as required for the complete burst. If MR1.ASM = 0, the MACSI device negates AB_AS in the last Td cycle. If MR1.ASM = 1, the MACSI device negates AB_AS in the first Td cycle.

Tr: MACSI device negates AB_R/W, AB_SIZ[2:0], releases AB_A and AB_AS, and stops driving AB_AD with data. Slave deasserts AB_ACK, AB_ERR, and AB_DEN.

7.0 Control Information

7.1 OVERVIEW

The Control Information includes Operation, Event, Status and Parameter Registers that are used to manage and operate the MACSI Device. A controller on the external Control Bus gains access to read and write these parameters via the Control Bus Interface.

The MACSI device combines the functions of the original DP83261 BMAC device and the DP83265 BSI device with many enhanced capabilities. The MACSI device has additional Control Bus address lines compared to the BMAC and BSI devices (CBA(8:0)). When the most significant address bit (CBA8) is zero, the internal BMAC register block is selected. When CBA8 is 1, the internal BSI register block is selected. The actual addresses within the MACSI device are defined in Table 7-1 and Table 7-2.

All registers and control bits within the BSI register block of the MACSI device have the same relative addresses and functions as they do in the BSI device. All registers and control bits within the BMAC register block of the MACSI device have the same relative addresses and functions as they do in the BMAC device. The only exceptions to this are shown in the detailed register descriptions following the memory map table. There are two registers which have new features unique to the MACSI device or functions which are slightly modified from the original BMAC or BSI device. These are MCMR0 and MCMR2.

TABLE 7-1. MACSI Memory Map (BMAC Registers)

Address	Register Name	Access Rules		Reset Value
		Read	Write	
000	MAC Mode Register 0 (MCMR0)	Always	Always	00
001	Option Register (Option)	Always	Always	00
002	Function Register (Function)	Always	Always	00
003	Reserved	N/A	N/A	
004	Reserved	N/A	N/A	
005	MAC Mode Register 2 (MCMR2)	Always	Always	00
006	Reserved	N/A	N/A	
007	MAC Revision (MCRev)	Always	Data Ignored	*
008	MAC Compare Register (MCCMP)	Always	Always	00
009–00B	Reserved	N/A	N/A	
00C	Current Receiver Status Register (CRS0)	Always	Data Ignored	00
00D	Reserved	N/A	N/A	
00E	Current Transmitter Status Register (CTS0)	Always	Data Ignored	00
00F	Reserved	N/A	N/A	
010	Ring Event Latch Register 0 (RELR0)	Always	Conditional	00
011	Ring Event Mask Register 0 (REMR0)	Always	Always	00
012	Ring Event Latch Register 1 (RELR1)	Always	Conditional	00
013	Ring Event Mask Register 1 (REMR1)	Always	Always	00
014	Token and Timer Event Latch Register (TELR0)	Always	Conditional	00
015	Token and Timer Event Mask Register (TEMR0)	Always	Always	00
016–017	Reserved	N/A	N/A	
018	Counter Increment Latch Register (CILR)	Always	Conditional	00
019	Counter Increment Mask Register (CIMR)	Always	Always	00
01A–01B	Reserved	N/A	N/A	
01C	Counter Overflow Latch Register (COLR)	Always	Conditional	00
01D	Counter Overflow Mask Register (COMR)	Always	Always	00
01E–027	Reserved	N/A	N/A	

TABLE 7-1. MACSI Memory Map (BMAC Registers) (Continued)

Address	Register Name	Access Rules		Reset Value
		Read	Write	
028	Internal Event Latch Register (IELR)	Always	Conditional	00
029-02B	Reserved	N/A	N/A	
02C	Exception Status Register (ESR)	Always	Conditional	00
02D	Exception Mask Register (EMR)	Always	Always	00
02E	Interrupt Condition Register (ICR)	Always	Data Ignored	00
02F	Interrupt Mask Register (IMR)	Always	Always	00
030-03F	Reserved	N/A	N/A	
040-07F	MAC Parameters	Stop Mode	Stop Mode	NA
080-0BF	Counters/Timers	Always	Stop Mode	NA
0C0-0FF	Reserved	N/A	N/A	

* = Contains a MAC Revision code.
NA = Not altered upon reset.
N/A = Not Applicable

Table 7-2. MACSI Memory Map (BSI Registers)

Address	Register Name	Access Rules		Reset Value
		Read	Write	
100	System Interface Mode Register 0 (SIMR0)	Always	Always	00
101	System Interface Mode Register 1 (SIMR1)	Always	Always	00
102	Pointer RAM Control and Address Register (PCAR)	Always	Always	NA
103	Mailbox Address Register (MBAR)	Always	Always	†
104	Master Attention Register (MAR)	Always	Data Ignored	00
105	Master Notify Register (MNR)	Always	Always	00
106	State Attention Register (STAR)	Always	Conditional	07
107	State Notify Register (STNR)	Always	Always	00
108	Service Attention Register (SAR)	Always	Conditional	0F
109	Service Notify Register (SNR)	Always	Always	00
10A	No Space Attention Register (NSAR)	Always	Conditional	FF
10B	No Space Notify Register (NSNR)	Always	Always	00
10C	Limit Address Register (LAR)	Always	Always	NA
10D	Limit Data Register (LDR)	Always	Always	NA
10E	Request Attention Register (RAR)	Always	Conditional	00
10F	Request Notify Register (RNR)	Always	Always	00
110	Request Channel 0 Configuration Register 0 (R0CR0)	Always	Always	NA
111	Request Channel 1 Configuration Register 0 (R1CR0)	Always	Always	NA
112	Request Channel 0 Expected Frame Status Register (R0EFSR)	Always	Always	NA
113	Request Channel 1 Expected Frame Status Register (R1EFSR)	Always	Always	NA

7.0 Control Information (Continued)

Table 7-2. MACSI Memory Map (BSI Registers)

Address	Register Name	Access Rules		Reset Value
		Read	Write	
114	Indicate Attention Register (IAR)	Always	Conditional	00
115	Indicate Notify Register (INR)	Always	Always	00
116	Indicate Threshold Register (ITR)	Always	INSTOP Mode or EXC = 1 Only	NA
117	Indicate Mode Configuration Register (IMCR)	Always	INSTOP Mode Only	NA
118	Indicate Copy Configuration Register (ICCR)	Always	Always	NA
119	Indicate Header Length Register (IHLR)	Always	INSTOP Mode or EXC = 1 Only	NA
11A	Address Configuration Register (ACR)	Always	Always	00
11B	Request Channel 0 Configuration Register 1 (R0CR1)	Always	Always	00
11C	Request Channel 1 Configuration Register 1 (R1CR1)	Always	Always	00
11D–11E	Reserved	N/A	N/A	
11F	System Interface Compare Register (SICMP)	Always	Always	NA
120–1FF	Reserved	N/A	N/A	

† = Initialized to a System Interface Revision code upon reset. The System Interface Revision code remains until it is overwritten by the host.

NA = Not altered upon reset.

N/A = Not Applicable

The MAC Control Information Address Space is divided into 4 groups as shown in Table 7-3. An information summary is given for each group followed by a detailed description of all registers.

- MAC Operation Registers (Table 7-4)
- MAC Event Registers (Table 7-5)
- MAC Parameters (Table 7-6)
- MAC Counters/Timers (Table 7-7)

The System Interface Operation registers are accessed directly via the Control Bus. Limit RAM Registers are accessed indirectly via the Control Bus using the Limit RAM Data and Limit RAM Address Registers. The Pointer RAM Registers are accessed indirectly via the Control Bus and ABus using the Pointer RAM Address and Control Register, the Mailbox Address Register, and a mailbox location in ABus memory. Descriptors are fetched (or written) by the MACSI device across the ABus.

- System Interface Registers (Table 7-8)

7.2 CONVENTIONS

When referring to multi-byte fields, byte 0 is always the most significant byte. When referring to bits within a byte, bit (7) is the most significant bit and bit (0) is the least significant bit. When referring to the contents of a byte, the most significant bit is always referred to first. When referring to a bit within a byte the notation register_name.bit_name is used. For example, MCMR0.RUN references the RUN bit in MAC Mode Register 0.

7.0 Control Information (Continued)

TABLE 7-3. MAC Control Information Address Space

Address Range	Description	Read Conditions	Write Conditions
000–007	Operation Registers	Always (Note 2)	Always (Note 2)
008–02F	Event Registers	Always (Note 2)	Always (cond) (Note 2)
030–03F	Reserved	N/A (Note 4)	N/A (Note 4)
040–07F	MAC Parameters	Stop Mode (Notes 1, 3)	Stop Mode (Notes 1, 3)
080-0BF	Counters/Timers	Always	Stop Mode (Note 1)
0C0-0FF	Reserved	N/A (Note 4)	N/A (Note 4)

Note 1: An attempt to access a currently inaccessible MAC Control location because of the current mode or because it is a reserved address space will cause a command error (bit CCE of the Exception Status Register is set to One).

Note 2: Read and write accesses to reserved locations within the Operation and Event Address ranges of the MAC Control Information Space cause a command error (bit CCE of the Exception Status Register is set to One).

Note 3: The MAC Parameter RAM is also accessible when conditions a, b and c are true. Otherwise accesses will cause a command error (bit CCE of the Exception Status Register is set to One) and the access will not be performed.
a) The MAC Transmitter is in state T0 or T1 or T3;
b) Option.ITC = 1 and Option.IRR = 1
c) Function.BCN = 0 and Function.CLM = 0

Note 4: Reserved bits in registers are always read as 0 and are not writable.

TABLE 7-4. MAC Operation Registers

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0	Read	Write
000	MCMR0	DIAG	ILB	RES	RES	PIP	MRP	CBP	RUN	Always	Always
001	Option	ITC	EMIND	IFCS	IRPT	IRR	ITR	ELA	ESA	Always	Always
002	Function	RES	RES	RES	CLM	BCN	MCRST	RES	MARST	Always	Always
003–004	Reserved	RES	RES	RES	RES	RES	RES	RES	RES	N/A	N/A
005	MCMR2	RES	RES	RES	RES	LLC MCE	SMT MCE	RES	BOSEL	Always	Always
006	Reserved	RES	RES	RES	RES	RES	RES	RES	RES	N/A	N/A
007	MCRev	REV(7–0)								Always	Ignored

Note 1: Attempts to access reserved locations within the MAC Operation Registers will result in Command Rejects (ESR.CCE set to ONE).

Note 2: On Master Reset, all MAC Operation Registers are set to Zero except the Revision Register.

TABLE 7-5. MAC Event Registers

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0	Read	Write
008	MCCMP	MCCMP(7–0)								Always	Always
009–00B	Reserved	RES	RES	RES	RES	RES	RES	RES	RES	N/A	N/A
00C	CRS0	RFLG	RS2	RS1	RS0	RES	RTS2	RTS1	RTS0	Always	Ignored
00D	Reserved	RES	RES	RES	RES	RES	RES	RES	RES	N/A	N/A
00E	CTS0	ROP	TS2	TS1	TS0	TTS3	TTS2	TTS1	TTS0	Always	Ignored
00F	Reserved	RES	RES	RES	RES	RES	RES	RES	RES	N/A	N/A
010	RELR0	RES	DUP ADD	PINV	OTR MAC	CLMR	BCNR	RNOP	ROP	Always	Conditional
011	REMR0	RES	DUP ADD	PINV	OTR MAC	CLMR	BCNR	RNOP	ROP	Always	Always
012	RELR1	LOCLM	HICLM	MYCLM	RES	RES	RES	MYBCN	OTRBCN	Always	Conditional
013	REMR1	LOCLM	HICLM	MYCLM	RES	RES	RES	MYBCN	OTRBCN	Always	Always
014	TELR0	RLVD	TKPASS	TKCAPT	CBERR	DUPTKR	TRTEXP	TVXEXP	ENTRMD	Always	Conditional
015	TEMR0	RLVD	TKPASS	TKCAPT	CBERR	DUPTKR	TRTEXP	TVXEXP	ENTRMD	Always	Always
016–017	Reserved	RES	RES	RES	RES	RES	RES	RES	RES	N/A	N/A
018	CILR	RES	TK RCVD	FR TRX	FR NCOP	FR COP	FR LST	FREI	FR RCV	Always	Conditional
019	CIMR	RES	TK RCVD	FR TRX	FR NCOP	FR COP	FR LST	FREI	FR RCV	Always	Always
01A–01B	Reserved	RES	RES	RES	RES	RES	RES	RES	RES	N/A	N/A
01C	COLR	RES	TK RCVD	FR TRX	FR NCOP	FR COP	FR LST	FREI	FR RCV	Always	Conditional
01D	COMR	RES	TK RCVD	FR TRX	FR NCOP	FR COP	FR LST	FREI	FR RCV	Always	Always
01E–027	Reserved	RES	RES	RES	RES	RES	RES	RES	RES	N/A	N/A
028	IELR	RES	RES	RES	RES	TSM ERR	RSM ERR	RES	MPE	Always	Conditional
029–02B	Reserved	RES	RES	RES	RES	RES	RES	RES	RES	N/A	N/A
02C	ESR	CWI	CCE	CPE	RES	RES	RES	RES	PPE	Always	Conditional
02D	EMR	ZERO	CCE	CPE	RES	RES	RES	RES	PPE	Always	Always
02E	ICR	ESE	IERR	RES	RES	COE	CIE	TTE	RNG	Always	Ignored
02F	IMR	ESE	IERR	RES	RES	COE	CIE	TTE	RNG	Always	Always
030–03F	Reserved	RES	RES	RES	RES	RES	RES	RES	RES	N/A	N/A

Note 1: Attempts to access reserved locations within the MAC Event Registers will result in Command Rejects (ESR.CCE set to ONE).

Note 2: Bits in the conditional write registers are only written when the corresponding bit in the Compare Register is equal to the bit to be overwritten.

Note 3: On Master Reset all Event Registers are reset to Zero.

7.3 ACCESS RULES

For the Ring Engine (MAC), all Control Interface accesses are checked against the current operational mode to determine if the register is currently accessible. If not currently accessible, the Control Bus Interface access is rejected (and reported in an Event Register). This means that the Control Bus Interface completes all accesses in a deterministic amount of time. Certain Status and Parameter registers are not accessible while in Run mode because the Ring Engine might access those locations. The Exception Status Register can be checked to verify that the operation terminated normally.

The Service Engine Registers are always accessible.

7.3.1 MAC Parameter RAM

The MAC parameter RAM is accessible in Stop mode and in RUN mode while: the MAC Transmitter is in states T0, T1 or T3; Option.ITC and Option.IRR are set; and Function.BCN and Function.CLM are not set. Otherwise a command reject is given (ESR.CCE) and the Parameter RAM will not be read or written.

TABLE 7-6. MAC Parameter RAM

Addr	Name	Register Contents
040	MLA0	MLA(47-40)
041	MLA1	MLA(39-32)
042	MLA2	MLA(31-24)
043	MLA3	MLA(23-16)
044	MLA4	MLA(15-8)
045	MLA5	MLA(7-0)
046	MSA0	MSA(15-8)
047	MSA1	MSA(7-0)
048	GLA0	GLA(47-40)
049	GLA1	GLA(39-32)
04A	GLA2	GLA(31-24)
04B	GLA3	GLA(23-16)
04C	GLA4	GLA(15-8)
04D	Reserved	
04E	GSA0	GSA(15-8)
04F	Reserved	
050	TREQ0	TREQ(31-24)
051	TREQ1	TREQ(23-16)
052	TREQ2	TREQ(15-8)
053	TREQ3	TREQ(7-0)
054	TBT0	TBT(31-24)
055	TBT1	TBT(23-16)
056	TBT2	TBT(15-8)
057	TBT3	TBT(7-0)
058	FGM0	FGM(7-0)
059	FGM1	FGM(F-8)
05A0-5F	Reserved	
060	PGM10	PGM(87-80)
061	PGM11	PGM(8F-88)
062	PGM12	PGM(97-90)
063	PGM13	PGM(9F-98)
064	PGM14	PGM(A7-A0)
065	PGM15	PGM(AF-A8)
066	PGM16	PGM(B7-B0)
067	PGM17	PGM(BF-B8)
068	PGM18	PGM(C7-C0)
069	PGM19	PGM(CF-C8)
06A	PGM1A	PGM(D7-D0)
06B	PGM1B	PGM(DF-D8)
06C	PGM1C	PGM(E7-E0)
06D	PGM1D	PGM(EF-E8)
06E	PGM1E	PGM(F7-F0)
06F	PGM1F	PGM(FF-F8)
070	PGM0	PGM(7-0)
071	PGM1	PGM(F-8)
072	PGM2	PGM(17-10)
073	PGM3	PGM(1F-18)
074	PGM4	PGM(27-20)
075	PGM5	PGM(2F-28)
076	PGM6	PGM(37-30)
077	PGM7	PGM(3F-38)
078	PGM8	PGM(47-40)
079	PGM9	PGM(4F-48)
07A	PGMA	PGM(57-50)
07B	PGMB	PGM(5F-58)
07C	PGMC	PGM(67-60)
07D	PGMD	PGM(6F-68)
07E	PGME	PGM(77-70)
07F	PGMF	PGM(7F-78)

7.3.2 MAC Counters/Timer Thresholds

The MAC event counters and timer thresholds are always readable, and are writable in Stop mode.

TABLE 7-7. MAC Counters and Timer Thresholds

Addr	Name	Register Contents
080–086	Reserved	
087	THSH1	Null(7–4), THSH1(3–0)
088–092	Reserved	
093	TMAX	Null(7–4), TMAX(3–0)
094–096	Reserved	
097	TVX	Null(7–4), TVX(3–0)
098	TNEG0	TNEG(31–24)
099	TNEG1	TNEG(23–16)
09A	TNEG2	TNEG(15–8)
09B	TNEG3	TNEG(7–0)
09C–09E	Reserved	
09F	LTCT	LTCT(7–0)
0A0	FRCT0	Zero(31–24)
0A1	FRCT1	Null(7–4), FRCT(19–16)
0A2	FRCT2	FRCT(15–8)
0A3	FRCT3	FRCT(7–0)
0A4	EICT0	Zero(31–24)
0A5	EICT1	Null(7–4), EICT(19–16)
0A6	EICT2	EICT(15–8)
0A7	EICT3	EICT(7–0)
0A8	LFCT0	Zero(31–24)
0A9	LFCT1	Null(7–4), LFCT(19–16)
0AA	LFCT2	LFCT(15–8)
0AB	LFCT3	LFCT(7–0)
0AC	FCCT0	Zero(31–24)
0AD	FCCT1	Null(7–4), FCCT(19–16)
0AE	FCCT2	FCCT(15–8)
0AF	FCCT3	FCCT(7–0)

Addr	Name	Register Contents
0B0	FNCT0	Zero(31–24)
0B1	FNCT1	Null(7–4), FNCT(19–16)
0B2	FNCT2	FNCT(15–8)
0B3	FNCT3	FNCT(7–0)
0B4	FTCT0	Zero(31–24)
0B5	FTCT1	Null(7–4), FTCT(19–16)
0B6	FTCT2	FTCT(15–8)
0B7	FTCT3	FTCT(7–0)
0B8	TKCT0	Zero(31–24)
0B9	TKCT1	Null(7–4), TKCT(19–16)
0BA	TKCT2	TKCT(15–8)
0BB	TKCT3	TKCT(7–0)
0BC	RLCT0	Zero(31–24)
0BD	RLCT1	Null(7–4), RLCT(19–16)
0BE	RLCT2	RLCT(15–8)
0BF	RLCT3	RLCT(7–0)

Note 1: Null(7–4) indicates that these bits are forced to zero on reads, and are ignored on writes.

Note 2: The value obtained on reads from reserved locations is not specified.

Note 3: On Master Reset, the event counters are not cleared.

The event counters are 20-bit counters and are read through three control accesses. In order to guarantee a consistent snapshot, whenever byte 3 of an event counter is read, byte 1 and byte 2 of the counters are loaded into a holding register. Byte 1 and byte 2 may then be read from the holding register. A single holding register is shared by all of the counters but (for convenience) is accessible at several places within the address space. Consistent readings across counters can be accomplished using the Counter Increment Latch Register (CILR).

The event counters are not reset as a result of a Master Reset. This may be done by either reading the counters out and keeping track relative to the initial value read, or by writing a value to all of the counters in stop mode. The counters may be written in any order. With some exceptions, interrupts are available when the counters increment or wraparound.

7.0 Control Information (Continued)

System Interface Registers

TABLE 7-8. System Interface Registers

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0	Read	Write
100	SIMR0	SMLB	SMLQ	VIRT	BIGEND	FLOW	MRST	FABCLK	TEST	Always	Always
101	SIMR1	AB_A31	AB_A30	AB_A29	AB_A28	ATM	ASM	RES	EAM	Always	Always
102	PCAR	BP1	BP0	PTRW	A4	A3	A2	A1	A0	Always	Always
103	MBAR	Mailbox Address [27:24], [23:16], [15:8], [7:0]								Always	Always
104	MAR	STA	NSA	SVA	RQA	INA	RES	RES	RES	Always	Ignored
105	MNR	STAN	NSAN	SVAN	RQAN	INAN	RES	RES	RES	Always	Always
106	STAR	ERR	BPE	CPE	CWI	CMDE	SPSTOP	RQSTOP	INSTOP	Always	Conditional
107	STNR	ERRN	BPEN	CPEN	CWIN	CMDEN	SPSTOPN	RQSTOPN	INSTOPN	Always	Always
108	SAR	RES	RES	RES	RES	ABR0	ABR1	LMOP	PTOP	Always	Conditional
109	SNR	RES	RES	RES	RES	ABR0N	ABR1N	LMOPN	PTOPN	Always	Always
10A	NSAR	NSR0	NSR1	LDI0	NSI0	LDI1	NSI1	LDI2	NSI2	Always	Conditional
10B	NSNR	NSR0N	NSR1N	LDI0N	NSI0N	LDI1N	NSI1N	LDI2N	NSI2N	Always	Always
10C	LAR	LRA3	LRA2	LRA1	LRA0	LMRW	RES	RES	LRD8	Always	Always
10D	LDR	LRD7	LRD6	LRD5	LRD4	LRD3	LRD2	LRD1	LRD0	Always	Always
10E	RAR	USRR0	RCMR0	EXCR0	BRKR0	USRR1	RCMR1	EXCR1	BRKR1	Always	Conditional
10F	RNR	USRR0N	RCMR0N	EXCR0N	BRKR0N	USRR1N	RCMR1N	EXCR1N	BRKR1N	Always	Always
110	R0CR0	TT1	TT0	PRE	HLD	FCT	SAT	VST	FCS	Always	Always
111	R1CR0	TT1	TT0	PRE	HLD	FCT	SAT	VST	FCS	Always	Always
112	R0EFSR	VDL	VFCS	EE1	EE0	EA1	EA0	EC1	EC0	Always	Always
113	R1EFSR	VDL	VFCS	EE1	EE0	EA1	EA0	EC1	EC0	Always	Always
114	IAR	RES	RES	EXCI0	BRKI0	EXCI1	BRKI1	EXCI2	BRKI2	Always	Conditional
115	INR	RES	RES	EXC0N	BRK0N	EXC1N	BRK1N	EXC2N	BRK2N	Always	Always
116	ITR	THR7	THR6	THR5	THR4	THR3	THR2	THR1	THR0	Always	INSTOP = 1 or EXC = 1 Only
117	IMCR	SM1	SM0	SKIP	FPP	BOT2	BOT1	BOB	BOS	Always	INSTOP = 1 Only
118	ICCR	CC0		RES	CC1		RES	CC2		Always	Always
119	IHLR	HL7	HL6	HL5	HL4	HL3	HL2	HL1	HL0	Always	INSTOP = 1 or EXC = 1 Only
11A	ACR	PCKI2	PCKI1	PCKI0	RSWP1	RSWP0	ISWP2	ISWP1	ISWP0	Always	Always
11B	R0CR1	EFT	RES	RES	RES	RES	RES	RES	ETR	Always	Always
11C	R1CR1	EFT	RES	RES	RES	RES	RES	RES	ETR	Always	Always
11D-11E	Reserved	RES	RES	RES	RES	RES	RES	RES	RES	N/A	N/A
11F	SICMP	CMP7	CMP6	CMP5	CMP4	CMP3	CMP2	CMP1	CMP0	Always	Always
120-1FF	Reserved	RES	RES	RES	RES	RES	RES	RES	RES	N/A	N/A

Note: Bits in the conditional write registers are only written when the corresponding bit in the System Interface Compare Register is equal to the bit to be overwritten.

7.0 Control Information (Continued)

Control Registers

The Control Registers are used to configure and control the operation of the MACSI device.

The Control Registers include the following registers:

- **MAC Mode Registers (MCMR2–0)** establish the major operating parameters for the MAC portion of the MACSI device.
- **Option Register (Option)** selects major configuration options for the MAC portion of the device.
- **Function Register (Function)** initiates major MAC level functions.
- **MAC Revision (MCRev)** this register contains the silicon revision code for the MAC state machines of this device.
- **System Interface Mode Registers (SIMR1–0)** establishes major operating parameters for the System Interface.
- **Pointer RAM Control and Address Register (PCAR)** is used to program the parameters for the PTOP (Pointer RAM Operation) service function.
- **Mailbox Address Register (MBAR)** is used to program the memory address of the mailbox used in the data transfer of the PTOP service function.
- **Limit Address Register (LAR)** is used to program the parameters and data used in the LMOP (Limit RAM Operation) service function.
- **Limit Data Register (LDR)** is used to program the data used in the LMOP service function.
- **Request Channel 0 Configuration Registers (R0CR1–0)** are used to program the operational parameters for Request Channel 0.
- **Request Channel 1 Configuration Registers (R1CR1–0)** are used to program the operational parameters for Request Channel 1.
- **Request Channel 0 Expected Frame Status Register (R0EFSR)** defines the expected frame status for frames being confirmed on Request Channel 0.
- **Request Channel 1 Expected Frame Status Register (R1EFSR)** defines the expected frame status for frames being confirmed on Request Channel 1.
- **Indicate Threshold Register (ITR)** is used to specify a maximum number of frames that can be copied onto an Indicate Channel before a breakpoint is generated.
- **Indicate Mode Configuration Register (IMCR)** specifies how the incoming frames are sorted onto Indicate Channels, enables frame filtering, and enables breakpoints on various burst boundaries.
- **Indicate Copy Configuration Register (ICCR)** is used to program the copy criteria for each of the Indicate Channels.
- **Indicate Header Length Register (IHLR)** defines the length of the frame header for use with the Header/Info Sort Mode.

Event Registers

The Event Registers record the occurrence of events or series of events. Events are recorded and contribute to generating Interrupt signals. There is a two-level hierarchy in generating this signal, as shown in *Figure 7-1.*

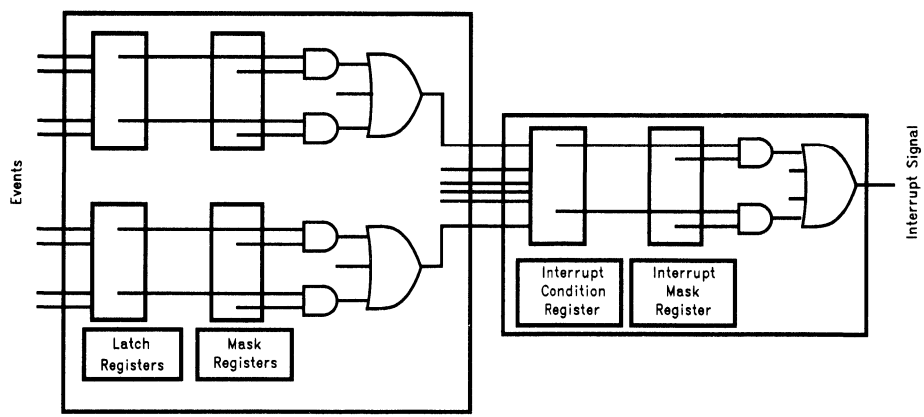

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FIGURE 7-1. Event Registers Hierarchy

7.0 Control Information (Continued)

The MACSI device has two interrupts signals. One provides interrupts on those events generated by the MAC state machines ($\overline{INT0}$) and the other provides interrupts on those events generated by the System Interface state machines ($\overline{INT1}$). This partition maintains hardware and software compatibility with earlier designs based on the BMAC and BSI devices.

At the first level of the hierarchy, events are recorded as bits in the Attention Registers (e.g., No Space Attention Register). Each Attention Register has a corresponding Notify Register (e.g., No Space Notify Register). When a bit in the Attention Register is set to One and its corresponding bit in the Notify Register is also set to One, the corresponding bit in the Master Attention Register will be set to one.

At the second level of the hierarchy, if a bit in the Master Attention Register is set to One and the corresponding bit in the Master Notify Register is set to One, the Interrupt signal is asserted.

To ensure that events are not missed when updating the attention registers, all attention registers are conditional write registers. Bits in Conditional Write Registers (e.g., No Space Attention Register) are only written when the corresponding bits in the Compare Register are equal to the bits to be overwritten. Read operations for conditional write registers automatically cause the Compare Register to be loaded with the contents of the conditional write register being accessed. The MACSI device contains two compare registers. One is used for Ring Engine Event Registers (MCCMP) and the other is used for System Interface Event Registers (SICMP).

Events are recorded in Attention Registers and contribute to the Interrupt when the bit in the corresponding Notify Register is set (see *Figure 7-1*). Bits in the Master Attention Register (MAR) are not cleared directly. They are cleared by clearing the lower level attention and/or notify register.

The Event Registers include the following registers:

- Ring Engine Event Registers ($\overline{INT0}$):
  - — MAC Compare Register (MCCMP)
  - — Current Receiver Status Register (CRS0)
  - — Current Transmitter Status Register (CTS0)
  - — Ring Event Latch Registers (RELR0–1)
  - — Ring Event Mask Registers (REMR0–1)
  - — Token and Timer Event Latch Register (TELR0)
  - — Token and Timer Event Mask Register (TEMR0)
  - — Counter Increment Latch Register (CILR)
  - — Counter Increment Mask Register (CIMR)
  - — Counter Overflow Latch Register (COLR)
  - — Counter Overflow Mask Register (COMR)
  - — Internal Event Latch Register (IELR)
  - — Exception Status Register (ESR)
  - — Exception Mask Register (EMR)
  - — Interrupt Condition Register (ICR)
  - — Interrupt Mask Register (IMR)
- Service Engine Event Registers ($\overline{INT1}$)
  - — Master Attention Register (MAR)
  - — Master Notify Register (MNR)
  - — State Attention Register (STAR)
  - — State Notify Register (STNR)
  - — Service Attention Register (SAR)
  - — Service Notify Register (SNR)
  - — No Space Attention Register (NSAR)
  - — No Space Notify Register (NSNR)
  - — Request Attention Register (RAR)
  - — Request Notify Register (RNR)
  - — Indicate Attention Register (IAR)
  - — Indicate Notify Register (INR)
  - — System Interface Compare Register (SICMP)

Servicing Interrupts

In the process of servicing an interrupt, the Host may use one or both levels of condition masks to disable new interrupts while one is being serviced. Soon after the Management Entity has processed the interrupt to some extent, it is ready to re-arm the interrupt in order to be notified of the next condition.

The Interrupt Control Register always contains the merged output of the masked Condition Registers as shown in *Figure 7-1*. It is only possible to remove a condition by setting the corresponding Condition Latch Register bit to Zero. By storing the events on-chip and having the ability to selectively set bits to Zero, the need for the software to maintain a copy of the Event Registers is eliminated.

To prevent the overwriting and consequent missing of events, an interlock mechanism is used. In the period between the Read of a Condition Latch Register and the corresponding Write to reset the condition, additional events can occur.

In order to prevent software from overwriting bits which have changed since the last read and losing interrupt events, a conditional write mechanism is employed. Only bits that have not changed since the last read can be written to a new value.

Whenever a Condition Latch Register is read, its contents are stored in the Compare Register. There is one Compare Register for the Ring Engine Event Registers and one Compare Register for the Service Engine Event Registers. Each bit of the Compare Register is compared with the current contents of the Register that is to be written. Writing a bit with a new value to a Condition Register is only possible when the corresponding bit in the Compare Register matches the bit in the Condition Register. For any bit that has not changed, the new value of the bit is written into the Register. For any bit that has changed, the writing of the bit is inhibited. The fact that an attempt was made to change a modified bit in the Register is latched in the Condition Write Inhibit bit in the Exception Status Register (ESR.CWI) for Ring Engine Registers and in the State Attention Register (STAR.CWI) for Service Engine Registers.

In the MACSI device, two Compare Registers are shared by all of the Condition Latch Registers (In the PLAYER+ device, there is a Compare Register for every Event Register). For the cases where more than one register must be read before writing a new value, the software may write the appropriate Compare Register with the most recently read value before writing the register again. Alternatively, the Event Register may be read again before being written.

7.0 Control Information (Continued)

7.4 RING ENGINE OPERATION REGISTERS

The Operation Registers are used to control the operation of the Ring Engine. The Operation Registers include the following registers

- MAC Mode Register (MCMR0, MCMR2)
- Option Register (Option)
- Function Register (Function)
- MAC Revision Register (MCRev)

MAC Mode Register 0 (MCMR0)

The Mode Register contains the current mode of the Ring Engine.

Access Rules

Address	Read	Write
000h	Always	Always

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
DIAG	ILB	RES	RES	PIP	MRP	CBP	RUN

Bit	Symbol	Description
D7	DIAG	**Diagnose Mode:** Enables access to all Ring Engine registers. When set, interoperability is not guaranteed. This bit should only be set when the Ring Engine is not inserted in a ring. **Design Note:** In diagnose mode, should an internal error occur the Current Receive and Transmit Status Registers are frozen with the error state until the internal state machine error condition is cleared (IELR.RSMERR and/or IELR.TSMERR).
D6	ILB	**Internal Loopback:** Enables the internal loopback that connects PRP, PRC, and PRD7–0 to PIP, PIC, and PID7–0 respectively. When enabled, the PHY Indicate Interface is ignored. Since the Ring Engine Transmitter and Receiver work as independent processes, a ring can be made operational in this mode, albeit consisting only of a single MAC. With an operational ring many diagnostic tests can be performed to test out MAC level and system level diagnostics including: the Beacon Process, the Claim Process, Ring Engine frame generation, token timers, event counters, transmission options, test of event detection capabilities, test of addressing modes, test of state machine sequencing options, etc. In addition, a large portion of the system interface logic can be tested, such as full duplex transmission to self within the limits of the system interface performance constraints, status handling and generation, etc. The same system tests can also be performed at different levels of loopback including through the various paths within a station, through the Configuration Switch of the PLAYER+ device, and through the Clock Recovery Module of the PLAYER+ device. System level tests can also be performed through the ring during normal operation.
D5–D4	RES	**Reserved**
D3	PIP	**PHY Indicate Parity:** Enables Odd Parity checking on the PHY Indicate Data pins (PID7–0). Parity errors are treated as code violations and cause the byte in error to be replaced with Idle symbols. When repeating, Parity is passed transparently from PIP to PRP. Odd Parity is generated for all internally generated fields. Odd Parity is always generated on the PHY Request Data pins (PRD7–0).
D2	MRP	**MAC Request Parity:** Enables Odd Parity checking on the MAC Request Data pins (MRD7–0). A parity error causes the transmission to be aborted. Odd parity is always generated on MIP.
D1	CBP	**Control Bus Parity:** Enables Odd Parity checking on the Control Bus Data pins (CBD7–0) during write operations. This applies to both the System Interface block and the Ring Engine (MAC) block. Parity errors detected while writing to a MAC register (CBA8 = 0) are reported in the CPE bit of the Exception Status Register (ESR 012Ch). Parity errors detected while writing to the System Interface block (CBA8 = 1) are reported in the CPE bit of the State Attention Register (STAR 106h). In either case, the write operation is inhibited. Parity is always generated on CBD7–0 during read accesses.
D0	RUN	**RUN/Stop:** 0: Stop Mode All state machines return to and remain in their zero state. All counters and timers are disabled. The Ring Engine transmits Idle symbols. 1: Run Mode. Enables operation as a MAC entity. The Ring Engine (MAC) must be in Run Mode to achieve an operational Ring.

7.0 Control Information (Continued)

Option Register (Option)

The Ring Engine supports several options. These options are typically static during operation but may be altered during operation. This register is initialized to Zero after a master reset.

Access Rules

Address	Read	Write
001h	Always	Always

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
ITC	EMIND	IFCS	IRPT	IRR	ITR	ELA	ESA

Bit	Symbol	Description
D7	ITC	**Inhibit Token Capture:** When enabled, the Ring Engine is prohibited from transmitting any (more) frames. This option prohibits entry to the Transmit Void and Data states from the Idle state, and causes exit from the Data state after the current frame has been transmitted. When enabled, it is still possible to perform Immediate transmissions from the transmitter Claim and Beacon states, but not from the Data state. This option can be used to temporarily block normal data service. It can also be used in conjunction with the Inhibit Recovery Required option to permit access via the Control Interface to the MAC Parameter RAM during MAC operation.
D6	EMIND	**External Matching Indicators:** Enables the setting of the transmitted A Indicator as an S symbol when the EA pin is set. This bit also enables the setting of the transmitted C Indicator as an S symbol when the internal VCOPY signal is asserted by the System Interface and the A Indicator is set as a result of an external match (i.e., the User asserts the EA pin). The Copied/Not Copied Frame Counters also increment as a result of external comparisons when this option is enabled.
D5	IFCS	**Implementer FCS:** Enables use of the standard CRC as the FCS on Implementer frames (FC.FF = 10). When enabled, Implementer frames are treated like all other frames. When Implementer frames are received with bad FCS and Er = R, the E Indicator is transmitted as S and EICT is incremented. On Implementer frames, the Standard does not mandate the setting of the E Indicator on the result of the FCS check. This allows Implementers to use alternate Frame Check Sequences aside from the standard 32-bit CRC. Implementers may also choose not to use any FCS in applications such as packet voice. If other stations in the ring are using Implementer frames with a non-standard FCS, this option may cause an interoperability problem.
D4	IRPT	**Inhibit Repeat:** When enabled, 1. the Ring Engine cannot enter the Transmitter Repeat and Issue_Token states. This causes all received PDUs to be stripped and prevents tokens from being issued. 2. Void frames are not transmitted during a service opportunity. 3. Idle to Repeat transition is inhibited and all received tokens and MAC frames except Lower—Claim and My_Beacon frames are ignored (Lower_Claim and My_Beacon frames may be ignored by setting Option.IRR). When the ring is operational, enabling this option causes the Reset actions to occur upon the completion of the service opportunity, if any. When the ring is not operational, Immediate Requests are serviced and continue to completion. The Inhibit Repeat option can be used to scrub the ring for a period longer than the Ring Latency. The option is also useful in non-FDDI applications to allow full duplex communication.

7.0 Control Information (Continued)

Bit	Symbol	Description
D3	IRR	**Inhibit Recovery Required:** When bit IRR is set to One, the Ring Engine does not take the transitions into the Claim state (T4). This option inhibits all the recovery required transitions as defined in the FDDI MAC Standard. This bit does not inhibit entry to the Tx__Claim state on a Claim Request generated at the MAC Request Interface via the Function Register. This option can be used to guarantee that implementation specific Beacon frames will be transmitted from the Tx__Beacon state. It is also useful in systems where Local Address Administration is used, to prohibit stations with the Null Address (or any address) from Claiming. The option could also be used to enable the use of the Ring Engine in non-FDDI full duplex applications (in conjunction with the Inhibit Repeat option) to disable the recovery timers.
D2	ITR	**Inhibit Token Release:** When bit ITR is set to One, the station will not issue a token after winning the Claim Process. The station remains in the Tx__Claim state while the station's Claim frames are returning to the station and it has won the Claim process. At this point the station is in control of the ring as long as no Higher__Claim or Beacon frames are received. While in control of the ring, the station may transmit special Claim or Management frames for a variety of implementation specific purposes. For example, the station might send out a Claim frame with a unique identifier to make sure that another station with its address and TREQ is not also Claiming.
D1	ELA	**Enable Long Addressing:** Enables the setting of A__Flag on matches of received Long Destination Addresses with MLA or any of the configured Group Addresses. Enables the setting of M__Flag and stripping on matches of received Long Source Address with MLA. Permits transmission of frames with Long Addresses. Frames with long addresses can be transmitted when long addressing is not enabled if the SA transparency option is selected. Claim and Beacon frames are sent with the Long Address if ELA is One. If ELA is Zero and ESA is One, Claim and Beacon frames are sent with the Short Address. When both ESA and ELA are Zero, the ring is effectively interrupted at this station. The token capture process and Error Recovery logic are suspended and no frames are repeated. Immediate requests are serviced if the SA Transparency option is selected.
D0	ESA	**Enable Short Addressing:** Enables the setting of A__Flag on matches of received Short Destination Addresses with MSA or any of the configured Group Addresses. Enables the setting of M__Flag and stripping on matches of received Short Source Addresses with MSA. Permits transmission of frames with Short Addresses. Frames with Short Addresses can be transmitted when Short Addressing is not enabled if the SA Transparency option is selected. Void frames are sent with the Short Address if ESA is set to One. If ESA is Zero and ELA is One, Void frames are sent with the Long Address. When both the ESA and ELA bits are Zero, the ring is effectively interrupted at this station. The token capture process and Error Recovery logic are suspended and no frames are repeated. Immediate requests are serviced if the SA Transparency option is selected.

7.0 Control Information (Continued)

Function Register (Function)

The Ring Engine performs the MAC Reset, Claim Request, and Beacon Request using the Function Register. The Register is initialized to Zero after a master reset. A function is performed by setting the appropriate bit to One. When the function is complete, the bit is cleared by the Ring Engine.

Access Rules

Address	Read	Write
002h	Always	Always

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
RES	RES	RES	CLM	BCN	MCRST	RES	MARST

Bit	Symbol	Description
D7–D5	RES	**Reserved**
D4	CLM	**Claim Request:** Produces the functions equivalent to an SM_CONTROL.request (Claim) and causes entry to the Tx_Claim State. The Ring Engine Transmitter is forced to enter the Tx_Claim State unless the Transmitter is in the Tx_Beacon State or bit BCN is set to One. Claim frames are then transmitted until the Claim process completes. The Claim process will not complete if Option.ITR = 1. A Claim Request is honored immediately from any state except the Beacon state. It is honored in the Beacon state when a My_Beacon returns. Claim requests are honored even when Option.IRR = 1. Claim frames are generated by the Ring Engine unless an Immediate Claim Request is available at the MAC Request Interface. Even with an Immediate Claim Request at the Interface, the Ring Engine transmits at least one Claim frame before the Claim frames from the MAC Request Interface are transmitted. If an external Claim frame is to be transmitted, the Claim frame should first be set up, then the request should be given to the MAC Request Interface before the CLM bit is set to One. The CLM bit is reset upon entry to the Claim or Beacon state.
D3	BCN	**Beacon Request:** Produces the functions of an SM_CONTROL.request (Beacon) as required by the FDDI MAC Standard. The Ring Engine Transmitter is forced to enter the Tx_Beacon State. Beacon frames are then transmitted until the Tx_Beacon Process completes. The Beacon Process will not complete if Option.IRR = 1. Beacon frames are generated by the Ring Engine unless an Immediate Beacon Request is present at the MAC Request Interface and a frame is ready to be transmitted. Even with an External Immediate Beacon Request the Ring Engine transmits at least one Beacon frame before the Beacon frames from the MAC Request Interface are transmitted. If an external Beacon frame is to be transmitted, the Beacon frame should first be set up via the System Interface and then bit BCN should be set to One. Setting this bit also sets bit D2 (MCRST). The BCN bit is cleared on entry to the Beacon state. If the User programs both D3 (BCN) and D4 (CLM) simultaneously, bit D3 (BCN) takes precedence.
D2	MCRST	**MAC Reset:** Forces the Receiver to state R0 (Listen) and the Transmitter to state T0 (Idle). TNEG (Registers 098–09B) is not loaded with TMAX (this operation can be performed as part of the MAC Reset Request actions by writing to TNEG Timers before the MAC Reset is initiated). MCRST takes precedence over bits D3 (BCN) and D4 (CLM), but does not clear these bits. A MAC Reset that occurs while a frame is being transmitted will cause the frame to be aborted. Frames without the Frame Status are not transmitted by the Ring Engine. Whenever the byte with the Ending Delimiter is transmitted, valid frame status is transmitted as well. If a MAC Reset occurs during the byte where the Ending Delimiter and E Indicator should be transmitted, it will not be transmitted. If a MAC Reset occurs on the cycle where the A and C Indicators are transmitted, they will still be transmitted.
D1	RES	**Reserved**
D0	MARST	**Master Reset:** A Master Reset is functionally equivalent to a hardware reset of the Ring Engine (MAC). A Master Reset sets all Ring Engine state machines and registers to default values. Master Reset causes the MCRST bit to be set. It also clears the Mode, Option, Event and Mask Registers. The Timers are set to their defaults. The Counters are not cleared. When the Master Reset function is complete, bit D0 (MARST) is set to Zero. At this time, all bits in the Function Register should be Zero.

7.0 Control Information (Continued)

MAC Mode Register 2 (MCMR2)

The Mode Register 2 (MCMR2) is used to program major operating parameters for the MAC portion of the MACSI device. This register should be programmed only at power-on, or after a software or hardware Master Reset.

This register is cleared upon reset.

Access Rules

Address	Read	Write
005h	Always	Always

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
RES	RES	RES	RES	LLC MCE	SMT MCE	RES	BOSEL

Bit	Symbol	Description
D4–D7	RES	**Reserved**
D3	LLC MCE	**LLC Multicast Enable (LLC MCE):** When this bit is set, the MACSI device will attempt to copy any LLC frame (as determined by the FC field) which also has the Individual/Group address bit set (i.e., is using a multicast address). The MAC block will not set the A or C indicators and the copied/not copied counters will not increment.
D2	SMT MCE	**SMT/MAC Multicast Enable (SMT MCE):** When this bit is set, the MACSI device will attempt to copy any SMT or MAC frame (as determined by the FC field) which also has the Individual/Group address bit set (i.e., is using a multicast address). The MAC block will not set the A or C indicators and the copied/not copied counters will not increment.
D1	RES	**Reserved**
D0	BOSEL	**Bridge Option Select (BOSEL):** This bit controls the interconnect of the STRIP and SAT signals from the System Interface block to the MAC block. When BOSEL = 0, the SAT output from the System Interface is connected to SAT input of the MAC. When BOSEL = 1, the STRIP output of the System Interface is connected to the SAT input of the MAC.

MAC Revision Register (MCRev)

The MAC Revision Register (MCRev) contains the revision number of the Ring Engine.

Access Rules

Address	Read	Write
007h	Always	Data Ignored

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0

Bit	Symbol	Description
D7–D0	REV(7–0)	**Revision Number:** Bits D7–D0 contain the version ID of the MAC State Machines. Software should consult this register for any software-specific issues related to the current version.

MAC Compare Register (MCCMP)

The Compare Register is written with the contents of a conditional event latch register when it is read. The Compare Register may also be written to directly.

Access Rules

Address	Read	Write
008h	Always	Always

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
CMP7	CMP6	CMP5	CMP4	CMP3	CMP2	CMP1	CMP0

Bit	Symbol	Description
D7–D0	CMP(7–0)	**Compare Register:** During a write to any of the conditional write registers in the Ring Engine (CBA8 = 0), CMP(7–0) are compared bitwise with bits D0–D7 of the accessed register. Only bits for which the comparison matches can be written to a new value. This function ensures that new events are not lost when clearing status for old events which the event handling has been completed.

7.0 Control Information (Continued)

Current Receiver Status Register (CRS0)

The Current Receiver Status Register (CRS0) records the status of the Receiver state machine. It is continuously updated. It remains stable when accessed.

When in Diagnose Mode, this register is frozen on an internal error until the internal error event is cleared by resetting the RSMERR bit in the Internal Event Latch Register.

Access Rules

Address	Read	Write
00Ch	Always	Data Ignored

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
RFLG	RS2	RS1	RS0	RES	RTS2	RTS1	RTS0

Bit	Symbol	Description
D7	RFLG	**R_Flag:** Current value of the Restricted Flag. When not holding the token indicates the type of the last valid token received. When holding the token indicates the type of token that will be issued at the end of the current service opportunity. 0: Non-Restricted 1: Restricted
D6–D4	RS(2–0)	**Receive State:** RS(2–0) represent the current state of the Receive state machine that implements the ANSI X3T9.5 standard MAC Receive Functions. The encoding is shown below. **RS2 RS1 RS0 Receive State** 0 0 0 Listen 0 0 1 Await_SD 0 1 0 RC_FR_CTRL (Receive FC) 0 1 1 RC_FR_BODY (Receive Frame Body) 1 0 0 RC_FR_STATUS (A and C Indicators) 1 0 1 CHECK_TOKEN (Check Token) 1 1 0 RC_FR_STATUS (Optional Indicators) 1 1 1 Reserved
D3	RES	**Reserved**
D2–D0	RTS(2–0)	**Receive Timing State:** RTS(2–0) represent the current state of the Receiver Timing state machine. The encoding is shown below. **RTS2 RTS1 RTS0 Receive Timing State** 0 0 0 Await_SD 0 0 1 Check_FC 0 1 0 Check_SA 0 1 1 Check_DA 1 0 0 Check_INFO 1 0 1 Check_MAC 1 1 x Reserved

7.0 Control Information (Continued)

Current Transmitter Status Register (CTS0)

The Current Transmitter Status Register (CTS0) records the status of the Transmitter state machine. It is continuously updated. It remains stable when accessed.

When in Diagnose Mode, this register is frozen on an internal error until the internal error event is cleared by resetting the TSMERR bit in the Internal Event Latch Register.

Access Rules

Address	Read	Write
00Eh	Always	Data Ignored

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
ROP	TS2	TS1	TS0	TTS3	TTS2	TTS1	TTS0

Bit	Symbol	Description
D7	ROP	**Ring Operational Flag:** Indicates the current value of the local Ring Operational Flag.
D6–D4	TS(2–0)	**Transmit State:** TS(2–0) represent the current state of the Transmit state machine that implements the ANSI X3T9.5 standard MAC Transmit Functions. The encoding is shown below.

TS2	TS1	TS0	Transmit State
0	0	0	Idle
0	0	1	Repeat
0	1	0	Data
0	1	1	Issue Token
1	0	0	Claim
1	0	1	Beacon
1	1	0	Reserved
1	1	1	Void

D3–D0 TTS(3–0)

Transmit Timing State: TTS(3–0) represent the current state of the Transmit Timing state machine. The encoding is shown below.

TTS3	TTS2	TTS1	TTS0	Transmit Timing State
0	0	0	0	Idle
0	0	0	1	Transmit Preamble
0	0	1	0	Wait for Data (FIFO)
0	0	1	1	Transmit SD and FC Fields
0	1	0	0	Transmit DA
0	1	0	1	Transmit SA
0	1	1	0	Transmit INFO
0	1	1	1	Transmit FCS
1	0	0	0	Transmit ED and FS
9h–Fh				Reserved

7.0 Control Information (Continued)

Ring Event Latch Register 0 (RELR0)

The Ring Event Latch Register 0 (RELR0) captures conditions that occur on the Ring including the receipt of Beacon and Claim frames, transitions in the Ring Operational flag, and the receipt of duplicate addresses. Each bit may be masked via the Ring Event Mask Register 0 (REMR0).

Access Rules

Address	Read	Write
010h	Always	Conditional

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
RES	DUPADD	PINV	OTRMAC	CLMR	BCNR	RNOP	ROP

Bit	Symbol	Description
D7	RES	**Reserved**
D6	DUPADD	**Duplicate Address Received:** Indicates that a valid individual frame addressed to this station was received with the A Indicator set. This could be caused by either a MAC using the same address (duplicate address) or a strip error at the Source (the frame was received twice).
D5	PINV	**PHY_Invalid Received:** Indicates that a PHY_Invalid was received. This could be the result of a PLAYER+ device Reset operation. PHY_Invalid causes the MAC Receiver to enter state R0 (Listen).
D4	OTRMAC	**Other MAC Frame Received:** Indicates that a MAC frame other than a Beacon or Claim frame was received. When set, restricted requests are not serviced.
D3	CLMR	**Claim Frame Received:** Indicates that a valid Claim frame was received. When set, restricted requests are not serviced. The type of Claim frame received is given in Register RELR1.
D2	BCNR	**Beacon Frame Received:** Indicates that a valid Beacon frame was received. When set, restricted and synchronous requests are not serviced. The type of Beacon frame received is given in Register RELR1.
D1	RNOP	**Ring Non-Operational Set:** Is set when the Local Ring Operational flag transitions from 1 to 0.
D0	ROP	**Ring Operational Set:** Is set when the Local Ring Operational flag transitions from 0 to 1.

7.0 Control Information (Continued)

Ring Event Mask Register 0 (REMR0)

The Ring Event Mask Register 0 (REMR0) is used to mask bits in Register RELR0. If a bit in Register REMR0 is set to One, the corresponding bit in Register RELR0 will be applied to the Interrupt Condition Register, which can then be used to generate an interrupt.

Access Rules

Address	Read	Write
011h	Always	Always

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
RES	DUPADD	PINV	OTRMAC	CLMR	BCNR	RNOP	ROP

Bit	Symbol	Description
D7	RES	**Reserved**
D6	DUPADD	**Duplicate Address Mask:** This bit is used to mask RELR0.DUPADD.
D5	PINV	**PHY__Invalid Mask:** This bit is used to mask RELR0.PINV.
D4	OTRMAC	**Other MAC Frame Mask:** This bit is used to mask RELR0.OTRMAC.
D3	CLMR	**Claim Frame Mask:** This bit is used to mask RELR0.CLMR.
D2	BCNR	**Beacon Frame Mask:** This bit is used to mask RELR0.BCNR.
D1	RNOP	**Ring Non-Operational Mask:** This bit is used to mask RELR0.RNOP.
D0	ROP	**Ring Operational Mask:** This bit is used to mask RELR0.ROP.

Ring Event Latch Register 1 (RELR1)

The Ring Event Latch Register 1 (RELR1) captures the progress of the Beacon and Claim processes. During the Beacon process, it records reception of an Other__Beacon or a My__Beacon. It also identifies Claim frames as Higher, Lower, or My Claim. Each bit may be masked via the Ring Event Mask Register 1 (REMR1).

Access Rules

Address	Read	Write
012h	Always	Conditional

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
LOCLM	HICLM	MYCLM	RES	RES	RES	MYBCN	OTRBCN

Bit	Symbol	Description
D7	LOCLM	**Lower__Claim Received:** Indicates that a Lower__Claim frame was received.
D6	HICLM	**Higher__Claim Received:** Indicates that a Higher__Claim frame was received.
D5	MYCLM	**My__Claim Received:** Indicates that a My__Claim frame was received. (This includes the comparison between the T__Bid__Rec and TREQ as specified in the standard.)
D4–D2	RES	**Reserved**
D1	MYBCN	**My__Beacon Received:** Indicates that a My__Beacon frame was received.
D0	OTRBCN	**Other__Beacon Received:** Indicates that an Other__Beacon frame was received.

7.0 Control Information (Continued)

Ring Event Mask Register 1 (REMR1)

Ring Event Mask Register 1 is used to mask bits in Register RELR1. If a bit in Register REMR1 is set to One, the corresponding bit in Register RELR1 will be applied to the Interrupt Condition Register, which can then be used to generate an interrupt to the CPU.

All bits in this register are set to Zero upon reset.

Access Rules

Address	Read	Write
013h	Always	Always

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
LOCLM	HICLM	MYCLM	RES	RES	RES	MYBCN	OTRBCN

Bit	Symbol	Description
D7	LOCLM	**Lower_Claim Mask:** This bit is used to mask RELR1.LOCLM.
D6	HICLM	**Higher_Claim Mask:** This bit is used to mask RELR1.HICLM.
D5	MYCLM	**My_Claim Mask:** This bit is used to mask RELR1.MYCLM.
D4–D2	RES	**Reserved**
D1	MYBCN	**My_Beacon Mask:** This bit is used to mask RELR1.MYBCN.
D0	OTRBCN	**Other_Beacon Mask:** This bit is used to mask RELR1.OTRBCN.

7.0 Control Information (Continued)

Token and Timer Event Latch Register 0 (TELR0)

The Token and Timer Event Latch Register 0 (TELR0) informs software of time expirations of the Token Rotation Timer (TRT) and Valid Transmission Timer (TVX). The TELR0 Register also reports token events such as duplicate token detection, restricted token reception, and general token capture and release. The completion of the Ring Latency measurement is also indicated in the TELR0 Register. Each bit may be masked via the Token and Timer Event Mask Register (TEMR0).

Access Rules

Address	Read	Write
014h	Always	Conditional

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
RLVD	TKPASS	TKCAPT	CBERR	DUPTKR	TRTEXP	TVXEXP	ENTRMD

Bit	Symbol	Description
D7	RLVD	**Ring Latency Valid:** 0: This bit is set to Zero to request a new latency value from the Ring Engine. The Ring Latency count is set to zero before each measurement. 1: This bit is set to One when the Ring Latency measurement is complete. This bit is written unconditionally and is not protected by the Compare Register. Note that if a duplicate of this station's MAC address exisits on the ring, the Ring Latency Measurement will not complete. The Ring Engine will restart the Ring Latency Measurement on each early Token arrival.
D6	TKPASS	**Token Passed:** Indicates that a valid token has been passed (without capturing it) or has been issued after a service opportunity.
D5	TKCAPT	**Token Captured:** Indicates that a token has been captured.
D4	CBERR	**Claim and/or Beacon Error:** Indicates that the Claim and/or Beacon Process failed because TRT expired while the Transmitter was in state T4 or T5.
D3	DUPTKR	**Duplicate Token Received:** Indicates that a valid token was received while the Transmitter was in state T2 or T3.
D2	TRTEXP	**TRT Expired:** Indicates that a valid token was not received within 2*TNEG.
D1	TVXEXP	**TVX Expired:** Indicates that a valid frame or token was not received in TVX time.
D0	ENTRMD	**Enter Restricted Mode:** Indicates that a Restricted Token was received and that the R__Flag transitions from 0 to 1.

7.0 Control Information (Continued)

Token and Timer Event Mask Register 0 (TEMR0)

The Token and Timer Event Mask Register 0 (TEMR0) is used to mask bits in Register TELR0. If a bit in Register TEMR0 is set to One, the corresponding bit in Register TELR will be applied to the Interrupt Condition Register, which can then be used to generate an interrupt.

All bits in this register are set to Zero upon reset.

Access Rules

Address	Read	Write
015h	Always	Always

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
RLVD	TKPASS	TKCAPT	CBERR	DUPTKR	TRTEXP	TVXEXP	ENTRMD

Bit	Symbol	Description
D7	RLVD	**Ring Latency Valid Mask:** This bit is used to mask TELR0.RLVD.
D6	TKPASS	**Token Passed Mask:** This bit is used to mask TELR0.TKPASS.
D5	TKCAPT	**Token Captured Mask:** This bit is used to mask TELR0.TKCAPT.
D4	CBERR	**Claim/Beacon Error Mask:** This bit is used to mask TELR0.CBERR.
D3	DUPTKR	**Duplicated Token Received Mask:** This bit is used to mask TELR0.DUPTKR.
D2	TRTEXP	**TRT Expired and Set Late_Flag Mask:** This bit is used to mask TELR0.TRTEXP.
D1	TVXEXP	**TVX Expired Mask:** This bit is used to mask TELR0.TVXEXP.
D0	ENTRMD	**Enter Restricted Mode Mask:** This bit is used to mask TELR0.ENTRMD.

7.0 Control Information (Continued)

Counter Increment Latch Register (CILR)

The Counter Increment Latch Register (CILR) records the occurrence of any increment to the SMT Counters in the Ring Engine. Each bit corresponds to a counter and is set when the corresponding counter is incremented. Each bit may be masked via the Counter Increment Mask Register (CIMR).

Access Rules

Address	Read	Write
018h	Always	Conditional

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
RES	TKRCVD	FRTRX	FRNCOP	FRCOP	FRLST	FREI	FRRCV

Bit	Symbol	Description
D7	RES	**Reserved**
D6	TKRCVD	**Token Received:** Is set when the Token Received Counter (TKCT) is incremented, indicating that a token has been received.
D5	FRTRX	**Frame Transmitted:** Is set when the Frame Transmitted Counter (FTCT) is incremented, indicating a frame has been transmitted.
D4	FRNCOP	**Frame Not Copied:** Is set when the Frame Not Copied Counter (FNCT) is incremented, indicating a frame could not be copied.
D3	FRCOP	**Frame Copied:** Is set when the Frame Copied Counter (FCCT) is incremented, indicating a frame has been copied.
D2	FRLST	**Frame Lost Isolated:** Is set when the Lost Frame Counter (LFCT) is incremented, indicating a format error has been detected in the frame.
D1	FREI	**Frame Error Isolated:** Is set when the Error Isolated Counter (EICT) is incremented, indicating an error has been isolated.
D0	FRRCV	**Frame Received:** Is set when the Frame Received Counter (FRCT) is incremented, indicating the reception of a frame.

7.0 Control Information (Continued)

Counter Increment Mask Register (CIMR)

The Counter Increment Mask Register (CIMR) is used to mask bits from the Counter Increment Latch Register (CILR). If a bit in Register CIMR is set to One, the corresponding bit in Register CILR will be applied to the Interrupt Condition Register, which can then be used to generate an interrupt to the CPU.

All bits in this register are set to Zero upon reset.

Access Rules

Address	Read	Write
019h	Always	Always

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
RES	TKRCVD	FRTRX	FRNCOP	FRCOP	FRLST	FREI	FRRCV

Bit	Symbol	Description
D7	RES	**Reserved**
D6	TKRCVD	**Token Received Counter Increment Mask:** This bit is used to mask CILR.TKRCVD.
D5	FRTRX	**Frame Transmitted Counter Increment Mask:** This bit is used to mask CILR.FRTRX.
D4	FRNCOP	**Frame Not Copied Counter Increment Mask:** This bit is used to mask CILR.FRNCOP.
D3	FRCOP	**Frame Copied Counter Increment Mask:** This bit is used to mask CILR.FRCOP.
D2	FRLST	**Lost Frame Counter Increment Mask:** This bit is used to mask CILR.FRLST.
D1	FREI	**Error Isolated Counter Increment Mask:** This bit is used to mask CILR.FREI.
D0	FRRCV	**Frame Received Counter Increment Mask:** This bit is used to mask CILR.FRRCV.

Counter Overflow Latch Register (COLR)

The Counter Overflow Latch Register (COLR) records carry events from the 20th bit of the SMT Counters in the Ring Engine. Each bit in the COLR corresponds to an individual counter. Each bit may be masked via the Counter Overflow Mask Register (COMR).

Access Rules

Address	Read	Write
01Ch	Always	Conditional

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
RES	TKRCVD	FRTRX	FRNCOP	FRCOP	FRLST	FREI	FRRCV

Bit	Symbol	Description
D7	RES	**Reserved**
D6	TKRCVD	**Token Received:** Is set to One when the Token Received Counter (TKCT) overflows.
D5	FRTRX	**Frame Transmitted:** Is set to One when the Frame Transmitted Counter (FTCT) overflows.
D4	FRNCOP	**Frame Not Copied:** Is set to One when the Frame Not Copied Counter (FNCT) overflows.
D3	FRCOP	**Frame Copied:** Is set to One when the Frame Copied Counter (FCCT) overflows.
D2	FRLST	**Frame Lost Isolated:** Is set to One when the Lost Frame Counter (LFCT) overflows.
D1	FREI	**Frame Error Isolated:** Is set to One when the Error Isolated Counter (EICT) overflows.
D0	FRRCV	**Frame Received:** Is set to One when the Frame Received Counter (FRCT) overflows.

Counter Overflow Mask Register (COMR)

The Counter Overflow Mask Register (COMR) is used to mask bits from the Counter Overflow Latch Register (COLR). If a bit in Register COMR is set to One, the corresponding bit in Register COLR will be applied to the Interrupt Condition Register, which can then be used to generate an interrupt to the CPU.

All bits in this register are set to Zero upon reset.

Access Rules

Address	Read	Write
01Dh	Always	Always

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
RES	TKRCVD	FRTRX	FRNCOP	FRCOP	FRLST	FREI	FRRCV

Bit	Symbol	Description
D7	RES	**Reserved**
D6	TKRCVD	**Token Received Counter Overflow Mask:** This bit is used to mask COLR.TKRCVD.
D5	FRTRX	**Frame Transmitted Counter Overflow Mask:** This bit is used to mask COLR.FRTRX.
D4	FRNCOP	**Frame Not Copied Counter Overflow Mask:** This bit is used to mask COLR.FRNCOP.
D3	FRCOP	**Frame Copied Counter Overflow Mask:** This bit is used to mask COLR.FRCOP.
D2	FRLST	**Lost Frame Counter Overflow Mask:** This bit is used to mask COLR.FRLST.
D1	FREI	**Error Isolated Counter Overflow Mask:** This bit is used to mask COLR.FREI.
D0	FRRCV	**Frame Received Counter Overflow Mask:** This bit is used to mask COLR.FRRCV.

Internal Event Latch Register (IELR)

The Internal Event Latch Register (IELR) reports internal errors in the Ring Engine. These errors include MAC Parity errors and inconsistencies in the Receiver and Transmitter state machines.

After an internal state machine error is detected and reported (bit RSMERR for the receiver and TSMERR for the transmitter), the Current Receive Status Register (CRS0) and Current Transmit Status Register (CTS0) continue to be updated as normal.

In Diagnose mode (Mode.Diag = 1), the Current Receive Status Register and Current Transmit Status Register are frozen with the errored state until the internal state machine error condition is cleared (bit RSMERR and/or TSMERR is set to Zero).

Errors internal to the Ring Engine cause a MAC_Reset.

Access Rules

Address	Read	Write
028h	Always	Conditional

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
RES	RES	RES	RES	TSM ERR	RSM ERR	RES	MPE

Bit	Symbol	Description
D7–D4	RES	**Reserved**
D3	TSMERR	**Transmit State Machine Error:** Indicates inconsistency in the Transmitter state machine. When set, causes bit MCRST of the Function Register to be set.
D2	RSMERR	**Receive State Machine Error:** Indicates inconsistency in the Receiver state machine. When set, causes bit MCRST of the Function Register to be set.
D1	RES	**Reserved**
D0	MPE	**MAC Interface Parity Error:** Indicates a Parity Error on the MAC Request Data pins (MRD7–0) when parity is enabled on the MA_Request Interface (bits MRP of the Mode Register are set and pin TXACK is asserted).

7.0 Control Information (Continued)

Exception Status Register (ESR)

The Exception Status Register (ESR) reports errors to the software. Errors include PHY Interface Parity Errors, illegal attempts to access currently inaccessible registers, and writing to a conditional write location if a register bit has changed since it was last read. Each bit may be masked via the Exception Mask Register (EMR).

Access Rules

Address	Read	Write
02Ch	Always	Conditional

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
CWI	CCE	CPE	RES	RES	RES	RES	PPE

Bit	Symbol	Description
D7	CWI	**Conditional Write Inhibit:** Indicates that at least one bit of the previous conditional write operation was not written. This bit is set unconditionally after each write to a conditional write register if the value of the Compare Register is not equal to the value of the register that was accessed for a write before it was written. This may indicate that the accessed register has changed since it was last read. This bit is cleared after a successful conditional write. This occurs when the value of the Compare Register is equal to the value of the register that was accessed for a write before it was written. CWI does not contribute to setting the ESE bit of the Interrupt Condition Register (it is always implicitly masked).
D6	CCE	**Control Bus Command Error:** Indicates that a Control Bus command was not performed due to an error, i.e., illegal command or a Control Bus Write Parity Error. An illegal command is an attempt to access a currently inaccessible register.
D5	CPE	**Control Bus Parity Error:** Indicates a Control Bus Parity Error was detected on the Control Bus Data pins (CBD7–0) during a write operation to a register. Parity errors are reported if parity is enabled on the Control Bus Interface (bit CBP of the Mode Register is set).
D4–D1	RES	**Reserved**
D0	PPE	**PHY Interface Parity Error:** Indicates parity error detected on PID7–0. Parity errors are reported when parity is enabled on the PHY_Request Interface (bit PIP of the Mode Register is set).

Exception Mask Register (EMR)

The Exception Mask Register (EMR) is used to mask bits in the Exception Status Register (ESR). If a bit in Register EMR is set to One, the corresponding bit in Register ESR will be applied to the Condition Register, which can then be used to generate an interrupt.

All bits in this register are set to Zero upon reset.

Access Rules

Address	Read	Write
02Dh	Always	Always

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
ZERO	CCE	CPE	RES	RES	RES	RES	PPE

Bit	Symbol	Description
D7	ZERO	**Zero:** This bit is always Zero. This implies that the CWI bit never contributes to the Interrupt Signal.
D6	CCE	**Control Bus Error Mask:** This bit is used to mask ESR.CCE.
D5	CPE	**Control Bus Parity Error Mask:** This bit is used to mask ESR.CPE.
D4–D1	RES	**Reserved**
D0	PPE	**PHY Interface Parity Error Mask:** This bit is used to mask ESR.PPE.

7.0 Control Information (Continued)

Interrupt Condition Register (ICR)

The Interrupt Condition Register (ICR) collects unmasked interrupts from the Event Registers. Interrupts are categorized into Ring Events, Token and Timer Events, Counter Events, and Error and Exceptional Status Events. If the bit in the Interrupt Mask Register (IMR) and the corresponding bit in the ICR are set to One, the INT0 pin is forced low and thus triggers an interrupt.

Note: Bits are cleared ONLY by clearing underlying conditions (Mask bit and/or Event Bit) in the appropriate Event Register.

Access Rules

Address	Read	Write
02Eh	Always	Data Ignored

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
ESE	IERR	RES	RES	COE	CIE	TTE	RNG

Bit	Symbol	Description
D7	ESE	**Exception Status Event Interrupt:** Is set if any unmasked bits in the Exception Status Register are set.
D6	IERR	**Internal Error Interrupt:** Is set if any bits in the Internal Event Register are set.
D5–D4	RES	**Reserved**
D3	COE	**Counter Overflow Event Interrupt:** Is set if any unmasked bits in the Counter Overflow Latch Register are set.
D2	CIE	**Counter Increment Event Interrupt:** Is set if any unmasked bits in the Counter Increment Latch Register are set.
D1	TTE	**Token and Timer Event Interrupt:** Is set if any unmasked bits in the Token and Timer Event Latch Register are set.
D0	RNG	**Ring Event Interrupt:** Is set if any unmasked bits in the Ring Event Latch Registers are set.

7.0 Control Information (Continued)

Interrupt Mask Register (IMR)

The Interrupt Mask Register (IMR) is used to mask bits in the Interrupt Condition Register (ICR). If a bit in Register IMR and the corresponding bit in Register ICR are set to One, the INT0 pin is forced low and causes an interrupt. Each bit in the IMR corresponds to an Event Register or a pair of Event Registers and associated bits.

Access Rules

Address	Read	Write
02Fh	Always	Always

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
ESE	IERR	RES	RES	COE	CIE	TTE	RNG

Bit	Symbol	Description
D7	ESE	**Exception Status Event Mask:** This bit is used to mask ICR.ESE.
D6	IERR	**Internal Error Mask:** This bit is used to mask ICR.IER.
D5–D4	RES	**Reserved**
D3	COE	**Counter Overflow Event Mask:** This bit is used to mask ICR.COE.
D2	CIE	**Counter Increment Event Mask:** This bit is used to mask ICR.CIE.
D1	TTE	**Token and Timer Event Mask:** This bit is used to mask ICR.TTE.
D0	RNG	**Ring Event Mask:** This bit is used to mask ICR.RNG.

7.0 Control Information (Continued)

7.5 MAC PARAMETERS

The MAC Parameters are accessible in the Stop Mode. These parameters are also accessible in the Run Mode when the following conditions are met:

a. the MAC Transmitter is in state T0, T1, or T3; and

b. bits ITC and IRR of the Option Register are set to One; and

c. bits CLM and BCN of the Function Register are set to Zero.

Otherwise read and write accesses will cause a command error (bit CCE of the Exception Status Register is set to One) and the access will not be performed.

The MAC Parameters are stored in the MAC Parameter RAM. They include the following control information:

- Individual Addresses: My Long Address (MLA0–5) and My Short Address (MSA0–1).
- Group Addresses: Group Long Address (GLA0–4) and Group Short Address (GSA0), Programmable Group Map (PGM0–F), and Fixed Group Map (FGM0–1).
- MAC Frame Information: Requested Target Token Rotation Time (TREQ0–3) and Transmit Beacon Type (TBT0–3)

7.5.1 Individual Addresses

The Ring Engine supports both Long and Short Individual Addresses simultaneously. The Station's Long Address is stored in registers MLA0–5. The Station's Short Address is stored in registers MSA0–1.

For received frames, MLA or MSA is compared with the received DA in order to set the Address recognized Flag (A__Flag) and compared with the received SA in order to set the My Address recognized Flag (M__Flag). In transmitted frames, MLA or MSA normally replaces the SA from the frame data stream (exception: when SA transparency is used).

Bits MLA(47) and MSA(15) are the most significant bits of the address and are transmitted and received first. Bits MLA(0) and MSA(0) are the least significant bits of the address and are transmitted and received last.

MLA and MSA should be valid for at least 12 byte times before the Addressing Mode is enabled and should remain valid for at least 12 byte times after the Addressing Mode is disabled in order to guarantee proper detection.

Bits ELA (Enable Long Addressing) and ESA (Enable Short Addressing) in the Option Register determine the address types that may be recognized and generated by this MAC.

My Long Address (MLA0–MLA5)

My Long Address (MLA0–MLA5) represent this station's long 48-bit address.

Access Rules

Address	Read	Write
040–045h	Stop Mode	Stop Mode

Register Bits

	D7	D6	D5	D4	D3	D2	D1	D0
MLA0	MLA(47)	MLA(46)	MLA(45)	MLA(44)	MLA(43)	MLA(42)	MLA(41)	MLA(40)
MLA1	MLA(39)	MLA(38)	MLA(37)	MLA(36)	MLA(35)	MLA(34)	MLA(33)	MLA(32)
MLA2	MLA(31)	MLA(30)	MLA(29)	MLA(28)	MLA(27)	MLA(26)	MLA(25)	MLA(24)
MLA3	MLA(23)	MLA(22)	MLA(21)	MLA(20)	MLA(19)	MLA(18)	MLA(17)	MLA(16)
MLA4	MLA(15)	MLA(14)	MLA(13)	MLA(12)	MLA(11)	MLA(10)	MLA(9)	MLA(8)
MLA5	MLA(7)	MLA(6)	MLA(5)	MLA(4)	MLA(3)	MLA(2)	MLA(1)	MLA(0)

Note: MLA(47) should always be set to 0.

My Short Address (MSA0–MSA1)

My Short Address (MSA0–MSA1) represent this station's short 16-bit address.

Access Rules

Address	Read	Write
046–047h	Stop Mode	Stop Mode

Register Bits

	D7	D6	D5	D4	D3	D2	D1	D0
MSA0	MSA(15)	MSA(14)	MSA(13)	MSA(12)	MSA(11)	MSA(10)	MSA(9)	MSA(8)
MSA1	MSA(7)	MSA(6)	MSA(5)	MSA(4)	MSA(3)	MSA(2)	MSA(1)	MSA(0)

Note: MSA(15) should always be set to 0.

7.0 Control Information (Continued)

7.5.2 Group Addresses

The Ring Engine supports detection of Group Addresses within programmable and fixed blocks of consecutive addresses. The algorithm used by the Ring Engine first performs a comparison between the most significant bits of the received DA with programmable and fixed addresses. If the most significant bits match, the remaining bits are used as an index into a programmable bit map. If the indexed bit is 1, the A_Flag is set to 1; if the indexed bit is 0, the A_Flag remains 0.

One programmable block of 256 group addresses is supported for group long addresses (GLA) and one programmable block of group addresses is supported for group short addresses (GSA). Both of the programmable ranges share the same programmable group address map (PGM).

For short addresses, the first byte of a received DA is compared with GSA0 (bits GSA(15–8)). If they match then the second byte is used as an index into the PGM. For long addresses the first 5 bytes of a received DA are compared with GLA0 through GLA4 (bits GLA(47–8)). If all 5 of these bytes match the corresponding byte in the received DA, then the 6th byte of the received DA is used as an index into the PGM. The last byte of the address is used as an index into the PGM in both long and short group addressing.

A fixed block of 16 group addresses is supported for both long and short addresses at the end of the address space that includes the Universal/Broadcast address (FF . . . FF). For short addresses, if the first 12 bits of the received DA are all 1's then the last 4 bits are used as an index into the 16-bit Fixed Group Map (FGM). Similarly, for long addresses if the first 44 bits are all 1's, the last 4 bits are also used as an index into the 16-bit FGM.

The Group Addresses should be valid for at least 12 byte times before the Addressing Mode is enabled and should remain valid for at least 12 byte times after the Addressing Mode is disabled in order to guarantee proper detection.

Bits ELA (Enable Long Addressing) and ESA (Enable Short Addressing) in the Option Register determine the address types that will be recognized by this MAC.

Alternative group addressing schemes may be implemented using external matching logic that monitors the byte stream at the PHY Interface. The result of the comparison is returned using the EA (External A_Flag) input signal.

Group Long Address (GLA0–GLA4)

Group Long Address (GLA0–GLA4) represents the first 5 bytes of the long address, bit GLA(47) to bit GLA(8).

To disable Long Group Address matches, bits GLA(46–8) should be set to all One's.

Access Rules

Address	Read	Write
048–04Ch	Stop Mode	Stop Mode

Register Bits

	D7	D6	D5	D4	D3	D2	D1	D0
GLA0	GLA(47)	GLA(46)	GLA(45)	GLA(44)	GLA(43)	GLA(42)	GLA(41)	GLA(40)
GLA1	GLA(39)	GLA(38)	GLA(37)	GLA(36)	GLA(35)	GLA(34)	GLA(33)	GLA(32)
GLA2	GLA(31)	GLA(30)	GLA(29)	GLA(28)	GLA(27)	GLA(26)	GLA(25)	GLA(24)
GLA3	GLA(23)	GLA(22)	GLA(21)	GLA(20)	GLA(19)	GLA(18)	GLA(17)	GLA(16)
GLA4	GLA(15)	GLA(14)	GLA(13)	GLA(12)	GLA(11)	GLA(10)	GLA(9)	GLA(8)

Note: GLA(47) should always be set to One.

Group Short Address (GSA0)

Group Short Address (GSA0) represents the station's short 16-bit address, bit GSA(15) to bit GSA(8).

It is possible to disable Short Group Addressing by programming bits GSA(14–8) to all Ones.

Access Rules

Address	Read	Write
04Eh	Stop Mode	Stop Mode

Register Bits

	D7	D6	D5	D4	D3	D2	D1	D0
GSA0	GSA(15)	GSA(14)	GSA(13)	GSA(12)	GSA(11)	GSA(10)	GSA(9)	GSA(8)

Note: GSA(15) is not used in the comparison since the comparison will only be accomplished if the received DA(15) is a One.

7.0 Control Information (Continued)

Fixed Group Address MAP (FGM0-FGM1)

If the first 44 bits of a long DA, DA(47-4), or the first 12 bits of a short DA, DA(15-4) are 1, the last 4 bits of the DA, DA(3-0), are used as an index into FGM.

The 4-bit index into FGM can be viewed in two different ways. It can be viewed as 4 bits selecting one of 16 bits where the hexadecimal equivalent of DA(3-0) can be used as the index. For example the broadcast address would index FGM(F). Alternatively it can be viewed as one bit, DA(3), selecting the byte (FGM0 or FGM1) and three bits, DA(2-0) selecting one of 8 bits within a byte.

Access Rules

Address	Read	Write
058-059h	Stop Mode	Stop Mode

Register Bits

	D7	D6	D5	D4	D3	D2	D1	D0
FGM0	FGM(7)	FGM(6)	FGM(5)	FGM(4)	FGM(3)	FGM(2)	FGM(1)	FGM(0)
FGM1	FGM(F)	FGM(E)	FGM(D)	FGM(C)	FGM(B)	FGM(A)	FGM(9)	FGM(8)

Bit FGM(F) must be set to One to ensure proper handling of frames with the Universal/Broadcast address including the SMT NSA frames. This is mandatory for interoperability on an FDDI Ring.

Programmable Group Address MAP (PGM0-PGM1F)

If the first 40 bits of a long DA, DA(47-8), match the GLA or the first 8 bits of a short DA, DA(15-8), match the GSA, the last 8 bits of the DA are used as an index into PGM.

The 8-bit index into PGM can be viewed in two different ways.

1. As 8 bits selecting one of 256 bits where the hexadecimal equivalent of DA(7-0) can be used as the index. For example a DA with the last byte as A2h indexes PGM(A2).
2. As 5 bits, DA(7-3), selecting the byte (PGM0 to PGM1F) and three bits, DA(2-0) selecting one of 8 bits within a byte. For example a DA with the last byte of A2h (1010 0010b) selects PGM14 bit 2.

It is possible to disable Long and Short Group Addressing by filling the Group Address Map with 0's.

In the MACSI device, PGM(00) to PGM(7F) are set equal to PGM(80) to PGM(FF) and are accessible via the Control Interface. This implies that DA(7) of group addresses is a don't care.

Access Rules

Address	Read	Write
070-07Fh	Stop Mode	Stop Mode

Register Bits

	D7	D6	D5	D4	D3	D2	D1	D0
PGM0	PGM(7)	PGM(6)	PGM(5)	PGM(4)	PGM(3)	PGM(2)	PGM(1)	PGM(0)
PGM1	PGM(F)	PGM(E)	PGM(D)	PGM(C)	PGM(B)	PGM(A)	PGM(9)	PGM(8)
PGM2	PGM(17)	PGM(16)	PGM(15)	PGM(14)	PGM(13)	PGM(12)	PGM(11)	PGM(10)
PGM3	PGM(1F)	PGM(1E)	PGM(1D)	PGM(1C)	PGM(1B)	PGM(1A)	PGM(19)	PGM(18)
PGM4	PGM(27)	PGM(26)	PGM(25)	PGM(24)	PGM(23)	PGM(22)	PGM(21)	PGM(20)
PGM5	PGM(2F)	PGM(2E)	PGM(2D)	PGM(2C)	PGM(2B)	PGM(2A)	PGM(29)	PGM(28)
PGM6	PGM(37)	PGM(36)	PGM(35)	PGM(34)	PGM(33)	PGM(32)	PGM(31)	PGM(30)
PGM7	PGM(3F)	PGM(3E)	PGM(3D)	PGM(3C)	PGM(3B)	PGM(3A)	PGM(39)	PGM(38)
PGM8	PGM(47)	PGM(46)	PGM(45)	PGM(44)	PGM(43)	PGM(42)	PGM(41)	PGM(40)
PGM9	PGM(4F)	PGM(4E)	PGM(4D)	PGM(4C)	PGM(4B)	PGM(4A)	PGM(49)	PGM(48)
PGMA	PGM(57)	PGM(56)	PGM(55)	PGM(54)	PGM(53)	PGM(52)	PGM(51)	PGM(50)
PGMB	PGM(5F)	PGM(5E)	PGM(5D)	PGM(5C)	PGM(5B)	PGM(5A)	PGM(59)	PGM(58)
PGMC	PGM(67)	PGM(66)	PGM(65)	PGM(64)	PGM(63)	PGM(62)	PGM(61)	PGM(60)
PGMD	PGM(6F)	PGM(6E)	PGM(6D)	PGM(6C)	PGM(6B)	PGM(6A)	PGM(69)	PGM(68)
PGME	PGM(77)	PGM(76)	PGM(75)	PGM(74)	PGM(73)	PGM(72)	PGM(71)	PGM(70)
PGMF	PGM(7F)	PGM(7E)	PGM(7D)	PGM(7C)	PGM(7B)	PGM(7A)	PGM(79)	PGM(78)

Access Rules

Address	Read	Write
060–06Fh	Stop Mode	Stop Mode

Register Bits

	D7	D6	D5	D4	D3	D2	D1	D0
PGM10	PGM(87)	PGM(86)	PGM(85)	PGM(84)	PGM(83)	PGM(82)	PGM(81)	PGM(80)
PGM11	PGM(8F)	PGM(8E)	PGM(8D)	PGM(8C)	PGM(8B)	PGM(8A)	PGM(89)	PGM(88)
PGM12	PGM(97)	PGM(96)	PGM(95)	PGM(94)	PGM(93)	PGM(92)	PGM(91)	PGM(90)
PGM13	PGM(9F)	PGM(9E)	PGM(9D)	PGM(9C)	PGM(9B)	PGM(9A)	PGM(99)	PGM(98)
PGM14	PGM(A7)	PGM(A6)	PGM(A5)	PGM(A4)	PGM(A3)	PGM(A2)	PGM(A1)	PGM(A0)
PGM15	PGM(AF)	PGM(AE)	PGM(AD)	PGM(AC)	PGM(AB)	PGM(AA)	PGM(A9)	PGM(A8)
PGM16	PGM(B7)	PGM(B6)	PGM(B5)	PGM(B4)	PGM(B3)	PGM(B2)	PGM(B1)	PGM(B0)
PGM17	PGM(BF)	PGM(BE)	PGM(BD)	PGM(BC)	PGM(BB)	PGM(BA)	PGM(B9)	PGM(B8)
PGM18	PGM(C7)	PGM(C6)	PGM(C5)	PGM(C4)	PGM(C3)	PGM(C2)	PGM(C1)	PGM(C0)
PGM19	PGM(CF)	PGM(CE)	PGM(CD)	PGM(CC)	PGM(CB)	PGM(CA)	PGM(C9)	PGM(C8)
PGM1A	PGM(D7)	PGM(D6)	PGM(D5)	PGM(D4)	PGM(D3)	PGM(D2)	PGM(D1)	PGM(D0)
PGM1B	PGM(DF)	PGM(DE)	PGM(DD)	PGM(DC)	PGM(DB)	PGM(DA)	PGM(D9)	PGM(D8)
PGM1C	PGM(E7)	PGM(E6)	PGM(E5)	PGM(E4)	PGM(E3)	PGM(E2)	PGM(E1)	PGM(E0)
PGM1D	PGM(EF)	PGM(EE)	PGM(ED)	PGM(EC)	PGM(EB)	PGM(EA)	PGM(E9)	PGM(E8)
PGM1E	PGM(F7)	PGM(F6)	PGM(F5)	PGM(F4)	PGM(F3)	PGM(F2)	PGM(F1)	PGM(F0)
PGM1F	PGM(FF)	PGM(FE)	PGM(FD)	PGM(FC)	PGM(FB)	PGM(FA)	PGM(F9)	PGM(F8)

7.5.3 Claim Information: Requested Target Token Rotation Time (TREQ)

The Requested Target Token Rotation Time is stored in registers TREQ0–TREQ3. TREQ(31–0) is represented as a negative two's complement number. This value is transmitted in all Claim frames generated by the Ring Engine.

Bits TREQ(31–24) are always transmitted as and compared with FFh and bits TREQ(7–0) are always transmitted as and compared with 00h, independent of the value stored in the MAC Parameter RAM. Bit TREQ(0) is transmitted last. TREQ is therefore programmable with 20.48 μs resolution and a maximum value of 1.34 seconds.

Access Rules

Address	Read	Write
050–053h	Stop Mode	Stop Mode

Register Bits

	D7	D6	D5	D4	D3	D2	D1	D0
TREQ0	TREQ(31)	TREQ(30)	TREQ(29)	TREQ(28)	TREQ(27)	TREQ(26)	TREQ(25)	TREQ(24)
TREQ1	TREQ(23)	TREQ(22)	TREQ(21)	TREQ(20)	TREQ(19)	TREQ(18)	TREQ(17)	TREQ(16)
TREQ2	TREQ(15)	TREQ(14)	TREQ(13)	TREQ(12)	TREQ(11)	TREQ(10)	TREQ(9)	TREQ(8)
TREQ3	TREQ(7)	TREQ(6)	TREQ(5)	TREQ(4)	TREQ(3)	TREQ(2)	TREQ(1)	TREQ(0)

7.5.4 Beacon Information: Transmit Beacon Type (TBT)

Transmit Beacon Type 0 (TBT0) represents the Transmit Beacon Type to be transmitted in the Information field of a Beacon frame. TBT1–TBT3 are not used by the Ring Engine.

When the Beacon state is reached as a result of a failed Claim process, the first byte of the Beacon Information field is forced to Zero to produce a Beacon Type 0 as required by the MAC Standard.

When the Beacon state is reached as a result of a Beacon Request (when Function.BCN is set), bits TBT(31–24) are transmitted as the Information field.

Access Rules

Address	Read	Write
054–057h	Stop Mode	Stop Mode

Register Bits

	D7	D6	D5	D4	D3	D2	D1	D0
TBT0	TBT(31)	TBT(30)	TBT(29)	TBT(28)	TBT(27)	TBT(26)	TBT(25)	TBT(24)
TBT1	TBT(23)	TBT(22)	TBT(21)	TBT(20)	TBT(19)	TBT(18)	TBT(17)	TBT(16)
TBT2	TBT(15)	TBT(14)	TBT(13)	TBT(12)	TBT(11)	TBT(10)	TBT(9)	TBT(8)
TBT3	TBT(7)	TBT(6)	TBT(5)	TBT(4)	TBT(3)	TBT(2)	TBT(1)	TBT(0)

7.6 TIMER VALUES

The Ring Engine stores several timer values and thresholds used in normal operation. With the exception of TNEG, the Timers use an exponential expansion on a 4-bit value to produce a negative twos complement 24-bit value used by the Timer Logic.

The Timer Values are always readable. These parameters are writable in Stop Mode.

The Timers include the following timers:

- Asynchronous Priority Threshold (THSH1)
- Maximum Token Rotation Time (TMAX)
- Valid Transmission Timer (TVX)
- Negotiated Target Rotation Time (TNEG0–3)

7.0 Control Information (Continued)

7.6.1 Asynchronous Priority Threshold (THSH1)

The Ring Engine currently supports one Asynchronous Priority Threshold in addition to the default threshold at TTRT. The Asynchronous Priority Threshold is used in a magnitude comparison with THT when an Asynchronous Priority Request is presented to the MAC Request Interface.

Bits 7–4 are always written to Zero and are always read as Zero.

When more than one threshold is used, the users of THSH1 have the lowest priority. All asynchronous transmissions are limited by TTRT. If the Late Flag is set, no frames may be transmitted, regardless of the value of the Asynchronous Priority Threshold.

Access Rules

Address	Read	Write
087h	Always	Stop Mode

Register Bits

	D7	D6	D5	D4	D3	D2	D1	D0
THSH1	Zero	Zero	Zero	Zero	THSH(3)	THSH(2)	THSH(1)	THSH(0)

THSH1(3–0)	Time remaining in THT when token becomes unusable
0	10.24 μs
1	20.48 μs
2	40.96 μs
3	81.92 μs
4	163.84 μs
5	327.68 μs
6	655.36 μs
7	1.3107 ms
8	2.6214 ms
9	5.2429 ms
A	10.486 ms
B	20.972 ms
C	41.943 ms (default)
D	83.886 ms
E	167.77 ms
F	335.54 ms

Warning: The default value may not be appropriate for all values of TNEG. In some cases, this could result in a request that is NEVER serviced.

7.0 Control Information (Continued)

7.6.2 Maximum Token Rotation Time (TMAX)

The Maximum Token Rotation Time (TMAX) denotes the maximum Target Token Rotation Time supported by this station. TMAX is stored as a 4-bit value that is expanded to a binary exponential value. Bits 7–4 are ignored during write operations and are always read as Zero.

TMAX has a maximum value of 1.34 seconds with a threshold of 40.96×2^{TMAX} μs. On a Master Reset (Function.MARST set to One), TMAX is set to the value of Ch which corresponds to 167.772 ms, the default specified by the FDDI MAC Standard.

For immediate transmissions from the transmit data state (T2), TMAX is always used to enforce an upper bound on the amount of time a station may transmit. TRT is reset to TMAX on entry to state T2 on immediate requests.

Access Rules

Address	Read	Write
093h	Always	Stop Mode

Register Bits

	D7	D6	D5	D4	D3	D2	D1	D0
TMAX	Zero	Zero	Zero	Zero	TMAX(3)	TMAX(2)	TMAX(1)	TMAX(0)

TMAX(3–0)	Time
0	40.96 μs
1	81.92 μs
2	163.84 μs
3	327.68 μs
4	655.36 μs
5	1.3107 ms
6	2.6214 ms
7	5.2429 ms
8	10.486 ms
9	20.972 ms
A	41.943 ms
B	83.886 ms
C	167.77 ms (default)
D	335.54 ms
E	671.09 ms
F	1.3422 s

7.0 Control Information (Continued)

7.6.3 Valid Transmission Time (TVX)

The Valid Transmission Timer (TVX) is used to increase the responsiveness of the ring to errors that cause ring recovery. The TVX value denotes the maximum time in which a valid frame or token should be seen by this station. TVX is stored as a 4-bit value that is expanded to a binary exponential value. Bits 7–4 are ignored during write operations and read as Zero.

TVX has a maximum value of 1.34 seconds with a threshold of 40.96×2^{TVX} μs. On a Master Reset TVX is set to the value of 6h which corresponds to 2.62 ms, the default specified by the FDDI MAC Standard.

Access Rules

Address	Read	Write
097h	Always	Stop Mode

Register Bits

	D7	D6	D5	D4	D3	D2	D1	D0
TVX	Zero	Zero	Zero	Zero	TVX(3)	TVX(2)	TVX(1)	TVX(0)

TVX(3–0)	Time
0	40.96 μs
1	81.92 μs
2	163.84 μs
3	327.68 μs
4	655.36 μs
5	1.3107 ms
6	2.6214 ms (default)
7	5.2429 ms
8	10.486 ms
9	20.972 ms
A	41.943 ms
B	83.886 ms
C	167.77 ms
D	335.54 ms
E	671.09 ms
F	1.3422 s

7.0 Control Information (Continued)

Negotiated Target Rotation Time (TNEG0–3)

The Negotiated Target Rotation Time (TNEG0–3) is a 32-bit twos complement value. It is the result of the Claim process. TNEG is loaded either directly from the received Claim Information field (T_Bid_Rc) or via the Control Interface.

The first byte of TNEG (bits TNEG(31–24)) always contains FFh. TNEG has a maximum value of 1.34 seconds and a resolution of 80 ns.

TRT is loaded with TNEG when the Ring_Operational flag is set. TNEG is not automatically compared with TREQ when the Ring_Operational flag is set. This should be checked by software whenever the ring becomes operational to make sure that TNEG is less than or equal to TREQ.

An implementation of the SM_Control.Request (Reset) should load TNEG with TMAX to remove any possibility of the station entering Claim early.

On a Master Reset (bit MARST in the Function Register is set), TNEG is set to FFE00000, which corresponds to 167.772 ms, the default TMAX specified by the FDDI MAC Standard.

Access Rules

Address	Read	Write
098–09Bh	Always	Stop Mode

Register Bits

	D7	D6	D5	D4	D3	D2	D1	D0
TNEG0	TNEG(31)	TNEG(30)	TNEG(29)	TNEG(28)	TNEG(27)	TNEG(26)	TNEG(25)	TNEG(24)
TNEG1	TNEG(23)	TNEG(22)	TNEG(21)	TNEG(20)	TNEG(19)	TNEG(18)	TNEG(17)	TNEG(16)
TNEG2	TNEG(15)	TNEG(14)	TNEG(13)	TNEG(12)	TNEG(11)	TNEG(10)	TNEG(9)	TNEG(8)
TNEG3	TNEG(7)	TNEG(6)	TNEG(5)	TNEG(4)	TNEG(3)	TNEG(2)	TNEG(1)	TNEG(0)

7.0 Control Information (Continued)

7.7 EVENT COUNTERS

The Event Counters are used to gain access to the internal 20-bit counters used to gather statistics.

The following event counters are included:

- Frame Received Counter (FRCT1–3)
- Error Isolated Counter (EICT1–3)
- Lost Frame Counter (LFCT1–3)
- Frame Copied Counter (FCCT1–3)
- Frame Not Copied Counter (FNCT1–3)
- Frame Transmitted Counter (FTCT1–3)
- Token Received Counter (TKCT1–3)
- Ring Latency Counter (RLCT1–3)
- Late Count Counter (LTCT)

7.7.1 Processing Procedures

The counters are 20-bit wrap-around counters except for the Late Count Counter which is a 4-bit sticky counter (see *Figure 7-2*).

Since the Control Bus Interface is an 8-bit interface and the counters are 20 bits wide, a register holding scheme is implemented. In order to provide a consistent snapshot of a counter, while the least significant byte is read, the upper 12 bits are loaded into a holding register which can then be read. The least significant byte must be read first.

The Counters are always readable and are writable in Stop Mode. The Counters are not reset as a result of a Master Reset. This may be done by either reading the Counters out and keeping track relative to the initial value read, or by writing a value (Zero) to all of the Counters in Stop Mode. The Counters may be written in any order. Interrupts may be requested when the counters increment (except for Ring Latency Counter) or wrap-around (except for Ring Latency Counter and Late Count Counter).

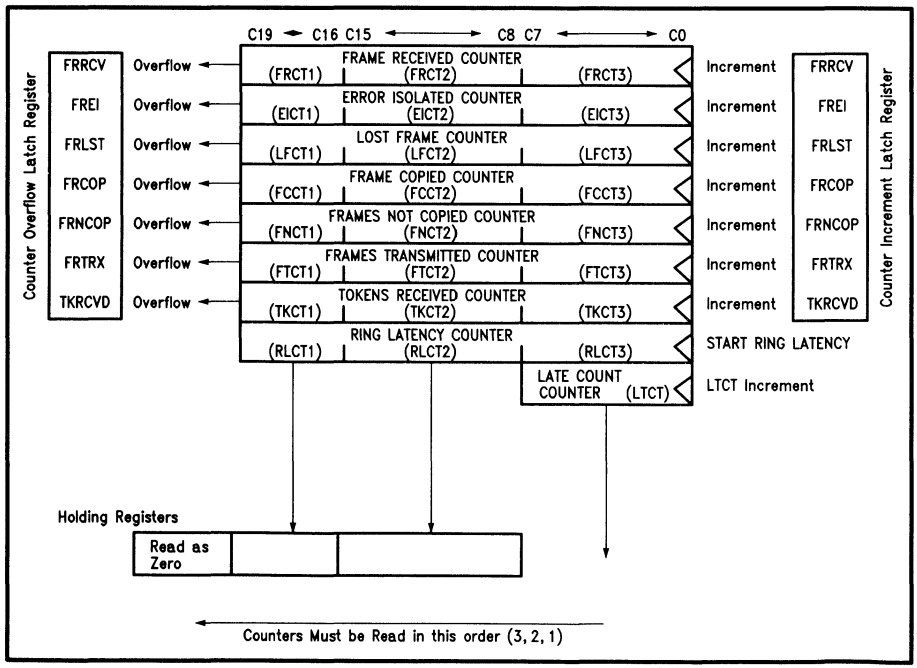

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FIGURE 7-2. Event Counters

7.0 Control Information (Continued)

Late Count Counter (LTCT)

The Late Count Counter (LTCT) is implemented differently than suggested by the FDDI MAC Standard, but provides similar information. The function of the Late Count Counter is divided between the Late_Flag and a separate counter. The Late_Flag is equivalent to the Standard Late Count with a non-zero value. It is maintained by the Ring Engine to indicate if it is possible to send asynchronous traffic. When the ring is operational, Late Count indicates the time it took the ring to recover the last time the ring went non-operational. When the ring is non-operational, Late Count indicates the time it has taken (so far) to recover the ring.

The Late Count is provided to assist Station Management in the isolation of serious ring errors. In many situations, it is helpful for SMT to know how long it has been since the ring went non-operational in order to determine if it is necessary to invoke recovery procedures. When the ring becomes non-operational, there is no way to know how long it will stay non-operational, therefore a timer is necessary. If the Late Count Counter is not provided, SMT would be forced to start a timer every time the ring goes non-operational even though it may seldom be used. By using the provided Late Count Counter, an SMT implementation may be able to alleviate this additional overhead.

The Late Count Counter is incremented every time TRT expires while the ring is non-operational and Late_Flag is set (once every TMAX). This counter is never writable, not even in Stop Mode. The counter is set to Zero as a result of a MAC Reset when a Beacon or Claim Request is not also present (Function.MCRST is set and Function.BCN and Function.CLM are not set) and every time the ring becomes non-operational. Late Count Counter is a sticky counter at 15.

Events reported in the Token and Timer Event Latch Register (TELR0.CBERR, TELR0.TRTEXP) can be used to determine that Late Count Counter has incremented. No overflow event is provided.

Access Rules

Address	Read	Write
09Fh	Always	N/A

Register Bits

	D7	D6	D5	D4	D3	D2	D1	D0
LTCT	Zero	Zero	Zero	Zero	CT3	CT2	CT1	CT0

7.0 Control Information (Continued)

Frame Received Counter (FRCT)

The Frame Received Counter (FRCT) is specified in the FDDI MAC Standard. It is the count of all complete frames received including MAC frames, Void frames and frames stripped by this station.

Interrupts are available on increment (CILR.FRRCV) and when the 20-bit counter overflows and wraps around (COLR.FRRCV).

Access Rules

Address	Read	Write
0A0–0A3h	Always	Stop Mode

Register Bits

	D7	D6	D5	D4	D3	D2	D1	D0
FRCT0	Zero	Zero	Zero	Zero	Zero	Zero	Zero	Zero
FRCT1	Zero	Zero	Zero	Zero	CT19	CT18	CT17	CT16
FRCT2	CT15	CT14	CT13	CT12	CT11	CT10	CT9	CT8
FRCT3	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0

Error Isolated Counter (EICT)

The Error Isolated Counter (EICT) is specified in the FDDI MAC Standard. It is the count of all error frames detected by this station and no previous station.

It is incremented when:

1. an FCS error is detected and the received Error Indicator (Er) is not equal to S; or
2. a frame of invalid length (i.e., off-boundary T) is received and Er is not equal to S; or
3. Er is not R or S

Interrupts are available on increment (CILR.FREI) and when the 20-bit counter overflows and wraps around (COLR.FREI).

Access Rules

Address	Read	Write
0A4–0A7h	Always	Stop Mode

Register Bits

	D7	D6	D5	D4	D3	D2	D1	D0
EICT0	Zero	Zero	Zero	Zero	Zero	Zero	Zero	Zero
EICT1	Zero	Zero	Zero	Zero	CT19	CT18	CT17	CT16
EICT2	CT15	CT14	CT13	CT12	CT11	CT10	CT9	CT8
EICT3	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0

7.0 Control Information (Continued)

Lost Frame Counter (LFCT)

The Lost Frame Counter (LFCT) is specified in the FDDI MAC Standard. It is the count of all instances where a Format Error is detected in a frame or token such that the credibility of the PDU reception is in doubt.

The Lost Frame Counter is incremented when any symbol other than a data or Idle symbol is received between the Starting and Ending Delimiters of a PDU (this includes parity errors).

Interrupts are available on increment (CILR.FRLST) and when the 20-bit counter overflows and wraps around (COLR.FRLST).

Access Rules

Address	Read	Write
0A8–0ABh	Always	Stop Mode

Register Bits

	D7	D6	D5	D4	D3	D2	D1	D0
LFCT0	Zero	Zero	Zero	Zero	Zero	Zero	Zero	Zero
LFCT1	Zero	Zero	Zero	Zero	CT19	CT18	CT17	CT16
LFCT2	CT15	CT14	CT13	CT12	CT11	CT10	CT9	CT8
LFCT3	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0

Frame Copied Counter (FCCT)

The Frame Copied Counter (FCCT) maintains the count of the number of frames addressed to this station and successfully copied. This counter can be used to accumulate station performance statistics.

The Frame Copied Counter is incremented when a frame which contains no errors and is addressed to this station is successfully copied. Copied MAC and Void frames are not included in this count.

When Option.EMIND is set, this count also includes frames copied as a result of external matches as indicated by EA.

For SMT NSA frames, the Frame Copied Count only increments for NSA frames received with the A Indicator as an R symbol for which the frame was copied. SMT NSA frames received with the A Indicator as an S symbol do not cause this count to increment, even if the frame is successfully copied.

Note that when in a promiscuous copy mode, this count will not increment for every frame copied, only for frames addressed to this station that are copied.

Interrupts are available on increment (CILR.FRCOP) and when the 20-bit counter overflows and wraps around (COLR.FRCOP).

Access Rules

Address	Read	Write
0AC–0AFh	Always	Stop Mode

Register Bits

	D7	D6	D5	D4	D3	D2	D1	D0
FCCT0	Zero	Zero	Zero	Zero	Zero	Zero	Zero	Zero
FCCT1	Zero	Zero	Zero	Zero	CT19	CT18	CT17	CT16
FCCT2	CT15	CT14	CT13	CT12	CT11	CT10	CT9	CT8
FCCT3	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0

7.0 Control Information (Continued)

Frame Not Copied Counter (FNCT)

The Frame Not Copied Counter (FNCT) maintains a count of the number of frames intended for this station that were not successfully copied by this station. This count can be used to accumulate station performance statistics such as insufficient buffering or deficient frame processing capabilities for frames addressed to this station.

The Frame Not Copied Counter is incremented when an internal match occurs on the Destination Address, no errors were detected in the frame, and the frame was not successfully copied (internal VCOPY signal not asserted by the System Interface). Not Copied MAC frames and Void frames are not included in this count.

When Option.EMIND is set this count also includes frames not copied on external matches indicated by EA.

The handling of SMT NSA frames follows the MAC-2 Draft Standard. For SMT NSA frames, the Frame Not Copied Count only increments for NSA frames received with the A Indicator as an R symbol for which the frame was not copied. SMT NSA frames received with the A Indicator as an S symbol do not cause this count to increment, even if the frame is not successfully copied.

Interrupts are available on increment (CILR.FRNCOP) and when the 20-bit counter overflows and wraps around (COLR.FRNCOP).

Access Rules

Address	Read	Write
0B0–0B3h	Always	Stop Mode

Register Bits

	D7	D6	D5	D4	D3	D2	D1	D0
FNCT0	Zero	Zero	Zero	Zero	Zero	Zero	Zero	Zero
FNCT1	Zero	Zero	Zero	Zero	CT19	CT18	CT17	CT16
FNCT2	CT15	CT14	CT13	CT12	CT11	CT10	CT9	CT8
FNCT3	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0

Frame Transmitted Counter (FTCT)

The Frame Transmitted Counter (FTCT) maintains the count of frames transmitted successfully by this station. The counter can be used to accumulate station performance statistics.

The Frame Transmitted Counter is incremented every time a complete frame is transmitted from the MAC Request Interface. MAC and Void frames generated by the Ring Engine are not included in the count.

Interrupts are available on increment (CILR.FRTRX) and when the 20-bit counter overflows and wraps around (COLR.FRTRX).

Access Rules

Address	Read	Write
0B4–0B7h	Always	Stop Mode

Register Bits

	D7	D6	D5	D4	D3	D2	D1	D0
FTCT0	Zero	Zero	Zero	Zero	Zero	Zero	Zero	Zero
FTCT1	Zero	Zero	Zero	Zero	CT19	CT18	CT17	CT16
FTCT2	CT15	CT14	CT13	CT12	CT11	CT10	CT9	CT8
FTCT3	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0

7.0 Control Information (Continued)

Token Received Counter (TKCT)

The Token Received Counter (TKCT) maintains the count of valid tokens received by this station. The counter can be used with the Ring Latency Counter to calculate the average network load over a period of time. The frequency of token arrival is inversely related to the network load.

The Token Received Counter is incremented every time a valid token arrives.

Interrupts are available on increment (CILR.TKRCVD) and when the 20-bit counter overflows and wraps around (COLR.TKRCVD).

Access Rules

Address	Read	Write
0B8–0BBh	Always	Stop Mode

Register Bits

	D7	D6	D5	D4	D3	D2	D1	D0
TKCT0	Zero	Zero	Zero	Zero	Zero	Zero	Zero	Zero
TKCT1	Zero	Zero	Zero	Zero	CT19	CT18	CT17	CT16
TKCT2	CT15	CT14	CT13	CT12	CT11	CT10	CT9	CT8
TKCT3	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0

Ring Latency Counter (RLCT)

The Ring Latency Counter (RLCT) is a measurement of time for PDUs to propagate around the ring. This counter contains the last measured ring latency whenever the RLVD bit of the Token and Timer Event Latch Register (TELR0.RLVD) is One.

The current ring latency is measured by timing the propagation of a My_Void frame around the ring. A new latency measurement can be requested by clearing the Ring Latency Valid bit of the Token Event Register (TELR0.RLVLD).

When the ring is operational, the next early token is captured. Before the token is re-issued, a My_Void frame is transmitted and the Ring Latency Counter (RLCT) is reset. The token will not be captured if the Inhibit Token Capture Option (Option.ITC) is set and the ring latency will not be measured.

When the ring is not operational, ring latency timing will commence at the end of the next immediate request. A My_Void is transmitted and RLCT is reset. This could be used to time how long the ring is non-operational since the My_Void frame will not return.

The Ring Latency Counter increments once every 6 byte times from when the Ending Delimiter of the My_Void frame is transmitted, until the Ending Delimiter of the My_Void frame returns. When the My_Void frame returns, the ring latency valid bit (TELR0.RLVLD) is set and may cause an interrupt. When set, RELR.RLVLD indicates that RLCT will be valid to within 1.28 μs. The Ring Latency Counter can measure ring latencies up to 1.3421772 seconds with accuracy of 1.28 μs.

The ring latency timing function is automatically disabled when exceptions are detected and retried at the next opportunity.

Since a Master Reset (Function.MARST) causes TELR0.RLVLD to be cleared, the ring latency will automatically be measured on the first opportunity (at the end of the first immediate request or with the first early token). Note that if a duplicate of this MAC address exists on the ring, the My_Void frame will be stripped and the ring latency measurement will never complete.

Access Rules

Address	Read	Write
0BC–0BFh	Always	Stop Mode

Register Bits

	D7	D6	D5	D4	D3	D2	D1	D0
RLCT0	Zero	Zero	Zero	Zero	Zero	Zero	Zero	Zero
RLCT1	Zero	Zero	Zero	Zero	CT19	CT18	CT17	CT16
RLCT2	CT15	CT14	CT13	CT12	CT11	CT10	CT9	CT8
RLCT3	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0

7.0 Control Information (Continued)

System Interface Mode Register 0 (SIMR0)

The System Interface Mode Register 0 (SIMR0) is used to program major operating parameters for the System Interface of the MACSI device. This register should be programmed only at power-on, or after a software Master Reset.

This register is cleared upon reset.

Access Rules

Address	Read	Write
100h	Always	Always

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
SMLB	SMLQ	VIRT	BIGEND	FLOW	MRST	FABCLK	TEST

Bit	Symbol	Description
D0	TEST	**Test Mode:** Enables test logic, in which the transmitted frames counter will cause a service loss after four frames, instead of 255 frames.
D1	FABCLK	**Fast ABus Clock:** Determines the metastability delay period for synchronizing between the ABus clock and the Ring clock (LBC). Upon reset this bit is cleared to Zero, which selects one ABus clock period as the delay. When this bit is set to One, only ½ of an ABus clock delay is used. When AB__CLK = LBC, (i.e., at 12.5 MHz and in phase), this bit should be set. For any AB__CLK greater than LBC, this bit must be Zero.
D2	MRST	**Master Reset:** When this bit is set, the indicate, Request, and Status/Space Machines are placed in Stop Mode, and System Interface registers are initialized to the values shown in Table 7-2. This bit is cleared after the reset is complete.
D3	FLOW	**Flow Parity:** When this bit is set, parity checking is enabled at the MAC Indicate Data (Receive Data) interface. The MACSI device uses Odd parity at all interfaces. Parity errors are reported in the STAR.BPE bit. Parity is never checked at the ABus interface. When this bit is set, the parity bit for each ABus data byte flows with the data byte through the internal FIFO and across the MAC Request (Transmit) interface where it is checked by the Ring Engine. Good parity is always generated on ABus. If this bit is reset, good parity is generated at the MAC Request interface. For the MAC Indicate Data interface, the parity check includes the frame's FC through ED fields. When this bit is Zero, no parity is checked on the MAC Indicate Data interface. In the BSI device, this bit also controlled the Control Bus Parity. In the MACSI device, Control Bus Parity is enabled using the MCMode.CBP bit (see "MAC Mode Register 0 (MCMR0)").
D4	BIGEND	**Big Endian Data Format:** Selects between the Little Endian (BIGEND = 0) or Big Endian (BIGEND = 1) data format. See *Figure 6-1.*
D5	VIRT	**Virtual Address Mode:** Selects between virtual (VIRT = 1) or physical (VIRT = 0) address mode on the ABus.
D6	SMLQ	**Small Queue:** Selects the size of all Descriptor queues and lists. When SMLQ = 0, the size is 4 kBytes; when SMLQ = 1, the size is 1 kBytes. Note that data pages are always 4 kBytes.
D7	SMLB	**Small Bursts:** Selects size of bursts on ABus. When SMLB = 0, the MACSI device uses 1-, 4-, and 8-word transfers. When SMLB = 1, the MACSI device uses 1- and 4-word transfers.

7.0 Control Information (Continued)

System Interface Mode Register1 (SIMR1)

The System Interface Mode Register 1 (SIMR1) is used to program major operating parameters for the System Interface of the MACSI device. This register should be programmed only at power-on, or after a software Master Reset.

This register is cleared upon reset. **Access Rules**

Address	Read	Write
101h	Always	Always

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
AB_A31	AB_A30	AB_A29	AB_A28	ATM	ASM	RES	EAM

Bit	Symbol	Description
D0	EAM	**Enhanced ABus Mode:** This bit controls the Enhanced ABus Mode (EAM). This enhanced mode is intended to reduce the amount of logic required to interface to the SBus. When this bit is reset, the ABus operates as it does on the original BSI device (normal ABus mode). When this bit is set, the AB_A(31:28) bits within this register are sourced on the upper nibble of the address/data lines during the address cycle. Read Data is strobed the cycle after the assertion of $\overline{AB\_ACK}$. The $\overline{AB\_BR}$ signal is guaranteed to be deasserted for at least two cycles (see *Figure 6-8* through *Figure 6-11*). The $\overline{AB\_DEN}$ pin becomes an input and the Error/Acknowledgment combinations are re-encoded.

EAM = 0		EAM = 1			
$\overline{AB\_ACK}$	$\overline{AB\_ERR}$	$\overline{AB\_ACK}$ Ack(2)*	$\overline{AB\_DEN}$ Ack(1)*	$\overline{AB\_ERR}$ Ack(0)*	Function
1	1	1	1	1	Wait Cycle
0	1	0	1	1	Word Acknowledgement
0	0	1	0	0	Retry
1	0	1	1	0	Error
		0	0	0	Not Supported
		0	0	1	Not Supported
		0	1	0	Not Supported
		1	0	1	Not Supported

D1	RES	**Reserved**
D2	ASM	**Address Strobe Mode:** The ASM bit controls the Address Strobe Mode. When this bit is reset, the $\overline{AB\_AS}$ signal operates as it does on the BSI device. When this bit is set, the MACSI device generates an $\overline{AB\_AS}$ signal which is designed to drive an address latch control line without additional logic (see *Figure 6-6* and *Figure 6-7*).
D3	ATM	**Address Timing Mode:** The ATM bit controls the Address Timing Mode. When this bit is reset, the AB_A(4:2) lines operate as they do on the BSI. These lines provide the demultiplexed address of the next word to be accessed on the ABus. When the ATM bit is set, the MACSI device provides the address of the *current* word being accessed on the ABus (see *Figure 6-6* and *Figure 6-7*). In order to use the de-multiplexed address pins AB_A(27:2), ATM must be set.
D7–D4	AB_A(31:28)	**AB_Address(31:28):** In normal operation (MR1.EAM = 0), the MACSI device encodes channel information on the upper nibble of the AB_AD bus during the address cycle. In Enhanced ABus mode (MR1.EAM = 1), the upper nibble of the address lines are driven with the data pattern which the user has stored in these four bits, AB_A(31:28).

7.0 Control Information (Continued)

Pointer RAM Control and Address Register (PCAR)

The Pointer RAM Control and Address Register (PCAR) is used to program the parameters for the PTOP (Pointer RAM Operation) service function, in which data is written to or read from a Pointer RAM Register.

This register is not altered upon reset.

Access Rules

Address	Read	Write
102h	Always	Always

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
BP1	BP0	PTRW	A4	A3	A2	A1	A0

Bit	Symbol	Description
D4–D0	A4–A0	**Pointer RAM Address:** These five bits contain the Pointer RAM Register address for a subsequent PTOP service function.
D5	PTRW	**PTOP Read/Write:** This bit determines whether a PTOP service function will be a read from the Pointer RAM Register to the mailbox in memory (PTRW = 1), or a write to the Pointer RAM Register from the mailbox (PTRW = 0).
D7–D6	BP1–BP0	**Byte Pointer:** These two bits are used to program an internal byte pointer for accesses to the 28-bit Mailbox Address Register. They are normally set to Zero to initialize the byte pointer for four successive writes (most-significant byte first) and are automatically incremented after each write. Because this register is not altered upon reset, it is important that these bits be explicitly configured before accessing the Mailbox Address Register.

Mailbox Address Register (MBAR)

The Mailbox Address Register (MBAR) is used to program the word-aligned 28-bit memory address of the mailbox used in the data transfer of the PTOP (Pointer RAM Operation) service function.

The address of the register is used as a window into four internal byte registers. The four byte registers are loaded by successive writes to the address after first setting the BP1–0 bits in the Pointer RAM Control and Address Register to Zero. The bytes must be loaded most-significant byte first. The MACSI device increments the byte pointer internally after each write or read. Mailbox Address bits 0 and 1 forced internally to Zero.

The four internal byte registers are initialized to a 28-bit System Interface Revision code upon reset. The System Interface Revision code remains until it is overwritten by the host. The BP1–0 bits in the PCAR must be initialized before accessing the MBAR to fetch the System Interface Revision code.

Access Rules

Address	Read	Write
103h	Always	Always

Register Bits

7	0
Mailbox Address [27:24]	
Mailbox Address [23:16]	
Mailbox Address [15:8]	
Mailbox Address [7:0]	

7.0 Control Information (Continued)

Master Attention Register (MAR)

The Master Attention Register (MAR) collects enabled attentions from the State Attention Register, Service Attention Register, No Space Attention Register, Request Attention Register, and Indicate Attention Register. If the Notify bit in the Master Notify Register and the corresponding bit in the MAR are set to One, the $\overline{INT1}$ pin is forced to LOW and thus triggers an interrupt.

Writes to the Master Attention Register are permitted, but do not change the contents.

All bits in this register are set to Zero upon reset.

Access Rules

Address	Read	Write
104h	Always	Data Ignored

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
STA	NSA	SVA	RQA	INA	RES	RES	RES

Bit	Symbol	Description
D2–D0	RES	**Reserved**
D3	INA	**Indicate Attention Register:** Is set if any bit in the Indicate Attention Register is set.
D4	RQA	**Request Attention Register:** Is set if any bit in the Request Attention Register is set.
D5	SVA	**Service Attention Register:** Is set if any bit in the Service Attention Register is set.
D6	NSA	**No Space Attention Register:** Is set if any bit in the No Space Attention Register is set.
D7	STA	**State Attention Register:** Is set if any bit in the State Attention Register is set.

Master Notify Register (MNR)

The Master Notify Register (MNR) is used to enable attentions in the Master Attention Register (MAR). If a bit in Register MNR and the corresponding bit in Register MAR are set to One, the INT1 signal is asserted to cause an interrupt.

All bits in this register are set to Zero upon reset.

Access Rules

Address	Read	Write
105h	Always	Always

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
STAN	NSAN	SVAN	RQAN	INAN	RES	RES	RES

Bit	Symbol	Description
D2–D0	RES	**Reserved**
D3	INAN	**Indicate Attention Register Notify:** This bit is used to enable the INA bit in Register MAR.
D4	RQAN	**Request Attention Register Notify:** This bit is used to enable the RQA bit in Register MAR.
D5	SVAN	**Service Attention Register Notify:** This bit is used to enable the SVA bit in Register MAR.
D6	NSAN	**No Space Attention Register Notify:** This bit is used to enable the NSA bit in Register MAR.
D7	STAN	**State Attention Register Notify:** This bit is used to enable the STA bit in Register MAR.

7.0 Control Information (Continued)

State Attention Register (STAR)

The State Attention Register (STAR) controls the state of the Indicate, Request, and Status/Space Machines. It also records parity, internal logic and ABus transaction errors. Each bit may be enabled by setting the corresponding bit in the State Notify Register.

This register is set to the value 07h upon reset.

Access Rules

Address	Read	Write
106h	Always	Conditional

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
ERR	BPE	CPE	CWI	CMDE	SPSTOP	RQSTOP	INSTOP

Bit	Symbol	Description
D0	INSTOP	**Indicate Stop:** This bit is set by the host to place the Indicate Machine in Stop Mode. It is also set upon reset. Three different conditions cause the MACSI device to set this bit. The first is an internal error. This is caused by a bad tag read out of the Indicate Data FIFO. This is a hardware error. The next condition is an invalid state. This is a hardware error where the Indicate Machine state bits contain an illegal pattern. The final condition is when the user programs an illegal header length for Header/Info sorting mode. An invalid value is any value less than four words. This bit is set by serious hardware failures or illegal software operations. Therefore it is recommended that the entire MACSI device be reset if this bit should get set during normal operation.
D1	RQSTOP	**Request Stop:** This bit is set by the host to place the Request Machine in Stop Mode. It is also set upon reset. The MACSI device will set this bit if it detects that the Request Machine has entered an illegal state. This is a hardware error. The MACSI device will also set this bit if an ABus error is detected during any Request Operation. This includes REQ, ODUD, and ODU fetches, and CNF writes. This bit is set by serious hardware failures or ABus errors. Therefore it is recommended that the entire MACSI device be reset if this bit should get set during normal operation
D2	SPSTOP	**Status/Space Stop:** This bit is set by the host to place the Status/Space Machine in Stop Mode. It is also set upon reset. In addition, the MACSI device will set this bit upon detecting an unrecoverable error. An unrecoverable error is an ABus error during a PSP fetch or a Pointer RAM Operation, (PTOP). In STOP Mode, only PTOP or LMOP service functions may be performed. This bit is set by ABus errors during critical Status/Space operations. Therefore it is recommended that the entire MACSI device be reset if this bit should get set during normal operation. This reset should include reloading of Pointer RAM values and restarting the PSP queues.
D3	CMDE	**Command Error:** Indicates that the host performed an invalid operation. This occurs when an invalid value is loaded into the Indicate Header Length Register (which also sets the INSTOP attention). This bit is cleared upon reset. This bit is set when software performs an illegal operation. This indicates either a software bug or the improper operation of the processor. Therefore it is recommended that the entire MACSI device be reset if this bit should get set during normal operation.
D4	CWI	**Conditional Write Inhibit:** Indicates that at least one bit of the previous conditional write operation was not written. This bit is set unconditionally after each write to a conditional write register. It is also set when the value of the Compare Register is not equal to the value of the register that was accessed for a write before it was written. This may indicate that the accessed register has changed since it was last read. This bit is cleared after a successful conditional write. CWI bit does not contribute to setting the STA bit of the Master Attention Register because its associated Notify bit is always 0. This bit is cleared upon reset.
D5	CPE	**Control Bus Parity Error:** Indicates a parity error detected on CBD7–0. If there is a Control Bus parity error during a host write, the write is suppressed. Control Bus parity errors are reported when flow-through parity is enabled (the FLOW bit of the Mode Register is set). This bit is cleared upon reset.
D6	BPE	**BMAC Device Parity Error:** Indicates parity error detected on MID7–0. This bit is cleared upon reset. This bit is only set if FLOW (parity enable) is set and the error occurred on a frame that the MACSI device has decided to copy or if it occurred before the copy decision was made.
D7	ERR	**Error:** This bit is set by the MACSI device when a non-recoverable error occurs. This includes any ABus transaction error or an internal state machine error. This bit is cleared upon reset.

7.0 Control Information (Continued)

State Notify Register (STNR)

The State Notify Register (STNR) is used to enable bits in the State Attention Register (STAR). If a bit in the STNR is set to One, the corresponding bit in Register STAR will be applied to the Master Attention Register, which can be used to generate an interrupt to the host.

All bits in this register are cleared to Zero upon reset.

Access Rules

Address	Read	Write
107h	Always	Always

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
ERRN	BPEN	CPEN	CWIN	CMDEN	SPSTOPN	RQSTOPN	INSTOPN

Bit	Symbol	Description
D0	INSTOPN	**Indicate Stop Notify:** This bit is used to enable the INSTOP bit in Register STAR.
D1	RQSTOPN	**Indicate Stop Notify:** This bit is used to enable the RQSTOP bit in Register STAR.
D2	SPSTOPN	**Status/Space Stop Notify:** This bit is used to enable the SPSTOP bit in Register STAR.
D3	CMDEN	**Command Error Notify:** This bit is used to enable the CMDE bit in Register STAR.
D4	CWIN	**Conditional Write Inhibit Notify:** This bit is always Zero. CWI is always masked.
D5	CPEN	**Control Bus Parity Error Notify:** This bit is used to enable the CPE bit in Register STAR.
D6	BPEN	**BMAC Device Parity Error Notify:** This bit is used to enable the BPE bit in Register STAR.
D7	ERRN	**Error Notify:** This bit is used to enable the ERR bit in Register STAR.

7.0 Control Information (Continued)

Service Attention Register (SAR)

The Service Attention Register (SAR) is used to present the attentions for the service functions. Each bit may be enabled by setting the corresponding bit in the State Notify Register.

This register is set to the value 0Fh upon reset.

Access Rules

Address	Read	Write
108h	Always	Conditional

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
RES	RES	RES	RES	ABR0	ABR1	LMOP	PTOP

Bit	Symbol	Description
D0	PTOP	**Pointer RAM Operation:** This bit is cleared by the host to cause the MACSI device to transfer data between a Pointer RAM Register and a predefined mailbox location in memory. The Pointer RAM Control and Address Register contains the Pointer RAM Register address and determines the direction of the transfer (read or write). The memory address is defined via the Mailbox Address Register. This bit is set by the MACSI device after it performs the data transfer. While PTOP = 0, the host must not alter the Pointer RAM Address and Control Register or the Mailbox Address Register.
D1	LMOP	**Limit RAM Operation:** This bit is cleared by the host to cause the MACSI device to transfer data between a Limit RAM Register and the Limit Data and Limit Address Registers. The Limit Address Register contains the Limit RAM Register address and determines the direction of the transfer (read and write). This bit is set by the MACSI device after it performs the data transfer. While LMOP = 0, the host must not alter either the Limit Address or Limit Data Register.
D2	ABR1	**Abort Request RCHN1:** This bit is cleared by the host to abort a Request on RCHN1. This bit is set by the MACSI device when RQABORT ends a request on RCHN1. The host may write a 1 to this bit, which may or may not prevent the request from being aborted. When this bit is cleared by the host, the USR1 bit in the Request Attention Register is set and further processing on RCHN1 is halted.
D3	ABR0	**Abort Request RCHN0:** This bit is cleared by the host to abort a Request on RCHN0. This bit is set by the MACSI device when RQABORT ends a request on RCHN0. The host may write a 1 to this bit, which may or may not prevent the request from being aborted. When this bit is cleared by the host, the USR0 bit in the Request Attention Register is set and further processing on RCHN0 is halted.
D7–D4	RES	**Reserved**

Service Notify Register (SNR)

The Service Notify Register (SNR) is used to enable attentions in the Service Attention Register (SAR). If a bit in Register SNR is set to One, the corresponding bit in Register SAR will be applied to the Master Attention Register, which can be used to generate a interrupt to the host.

All bits in this register are set to Zero upon reset.

Access Rules

Address	Read	Write
109h	Always	Always

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
RES	RES	RES	RES	ABRON	ABR1N	LMOPN	PTOPN

Bit	Symbol	Description
D0	PTOPN	**Pointer RAM Operation Notify:** This bit is used to enable the PTOP bit in Register SAR.
D1	LMOPN	**Limit RAM Operation Notify:** This bit is used to enable the LMOP bit in Register SAR.
D2	ABR1N	**Abort Request RCHN1 Notify:** This bit is used to enable the ABR1 bit in Register SAR.
D3	ABR0N	**Abort Request RCHN0 Notify:** This bit is used to enable the ABR0 bit in Register SAR.
D4–D7	RES	**Reserved**

7.0 Control Information (Continued)

No Space Attention Register (NSAR)

The No Space Attention Register (NSAR) presents the attentions generated when the CNF, PSP, or IDUD Queues run out of space. The host may set any attention bit to cause an attention for test purposes only, though this should not be done during normal operation.

The No Data Space attentions are set and cleared by the MACSI device automatically. The No Status Space attentions are set by the MACSI device, and must be cleared by the host.

Upon reset this register is set to 0xff.

Access Rules

Address	Read	Write
10Ah	Always	Conditional

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
NSR0	NSR1	LDI0	NSI0	LDI1	NSI1	LDI2	NSI2

Bit	Symbol	Description
D0	NSI2	**No Status Space on ICHN2:** This bit is set by the MACSI device upon a Reset, or when an IDUD has been written to the next-to-last available entry in the Indicate Channel's IDUD Status Queue. When this occurs, the MACSI device stops copying on ICHN2 and the last IDUD is written with special status. This bit must be cleared by the host before the MACSI device will resume copying on this Channel. Note that this bit should only be cleared after the appropriate limit register has been updated to give the MACSI more status space.
D1	LDI2	**Low Data Space on ICHN2:** This bit is set by the MACSI device upon Reset, or when a PSP is prefetched from ICHN2's last PSP Queue location (as defined by the PSP Queue Limit Register). Note that the amount of warning is dependent on the length of the frame. There will always be one more page (4 kBytes) available for the MACSI device when this attention is generated. Another FDDI maximum-length frame (after the current one) will not fit in this space. If PSP fetching was stopped because there were no more PSP entries, fetching will resume automatically when the PSP Queue Limit Register is updated. This bit will be cleared automatically when the new PSP Descriptors are fetched. This bit should never be cleared directly by software. Clearing this bit can cause the MACSI device to fetch invalid PSP descriptors.
D2	NSI1	**No Status Space on ICHN1:** This bit is set by the MACSI device upon a Reset, or when an IDUD has been written to the next-to-last available entry in the Indicate Channel's IDUD Status Queue. When this occurs, the MACSI device stops copying on ICHN1 and the last IDUD is written with special status. This bit must be cleared by the host before the MACSI device will resume copying on this Channel. Note that this bit should only be cleared after the appropriate limit register has been updated to give the MACSI device more status space.
D3	LDI1	**Low Data Space on ICHN1:** This bit is set by the MACSI device upon Reset, or when a PSP is prefetched from ICHN1's last PSP Queue location (as defined by the PSP Queue Limit Register). Note that the amount of warning is dependent on the length of the frame. There will always be one more page (4 kBytes) available for the MACSI device when this attention is generated. Another FDDI maximum-length frame (after the current one) will not fit in this space. If PSP fetching was stopped because there were no more PSP entries, fetching will resume automatically when the PSP Queue Limit Register is updated. This bit will be cleared automatically when the new PSP Descriptors are fetched. This bit should never be cleared directly by software. Clearing this bit can cause the MACSI device to fetch invalid PSP descriptors.

Bit	Symbol	Description
D4	NSI0	**No Status Space on ICHN0:** This bit is set by the MACSI device upon a Reset, or when an IDUD has been written to the next-to-last available entry in the Indicate Channel's IDUD Status Queue. When this occurs, the MACSI device stops copying on ICHN0 and the last IDUD is written with special status. This bit must be cleared by the host before the MACSI device will resume copying on this Channel. Note that this bit should only be cleared after the appropriate limit register has been updated to give the MACSI device more status space.
D5	LDI0	**Low Data Space on ICHN0:** This bit is set by the MACSI device upon Reset, or when a PSP is prefetched from ICHN0's last PSP Queue location (as defined by the PSP Queue Limit Register). Note that the amount of warning is dependent on the length of the frame. There will always be one more page (4 kBytes) available for the MACSI device when this attention is generated. Another FDDI maximum-length frame (after the current one) will not fit in this space. If PSP fetching was stopped because there were no more PSP entries, fetching will resume automatically when the PSP Queue Limit Register is updated. This bit will be cleared automatically when the new PSP Descriptors are fetched. This bit should never be cleared directly by software. Clearing this bit can cause the MACSI device to fetch invalid PSP descriptors.
D6	NSR1	**No Status Space on RCHN1:** This bit is set by the MACSI device upon a Reset, or when it has written a CNF Descriptor to the next-to-last Queue location. Due to internal pipelining, the MACSI device may write up to two more CNFs to the Queue after this attention is generated. Thus the Host must set the CNF Queue Limit Register to be one less than the available space in the Queue. This bit (as well as the USR attention bit) must be cleared by the Host before the MACSI device will continue to process requests on RCHN1. Note that this bit should only be cleared after the appropriate limit register has been updated to give the MACSI device more status space.
D7	NSR0	**No Status Space on RCHN0:** This bit is set by the MACSI device upon Reset, or when it has been written a CNF Descriptor to the next-to-last Queue location. Due to internal pipelining, the MACSI device may write up to two more CNFs to the Queue after this attention is generated. Thus the Host must set the CNF Queue Limit Register to be one less than the available space in the Queue. This bit (as well as the USR attention bit) must be cleared by the Host before the MACSI device will continue to process requests on RCHN0. Note that this bit should only be cleared after the appropriate limit register has been updated to give the MACSI device more status space.

7.0 Control Information (Continued)

No Space Notify Register (NSNR)

The No Space Notify Register (NSNR) is used to enable attentions in the No Space Attention Register (NSAR). If a bit in Register NSNR is set to One, the corresponding bit in Register NSAR will be applied to the Master Attention Register, which can be used to generate an interrupt to the host.

All bits in this register are set to Zero upon reset.

Access Rules

Address	Read	Write
10Bh	Always	Always

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
NSR0N	NSR1N	LDI0N	NSI0N	LDI1N	NSI1N	LDI2N	NSI2N

Bit	Symbol	Description
D0	NSI2N	**No Status Space on ICHN2 Notify:** This bit is used to enable the NSI2 bit in Register NSAR.
D1	LDI2N	**Low Data Space on ICHN2 Notify:** This bit is used to enable the LDI2 bit in Register NSAR.
D2	NSI1N	**No Status Space on ICHN2 Notify:** This bit is used to enable the NSI1 bit in Register NSAR.
D3	LDI1N	**Low Data Space on ICHN2 Notify:** This bit is used to enable the LDI1 bit in Register NSAR.
D4	NSI0N	**No Status Space on ICHN2 Notify:** This bit is used to enable the NSI0 bit in Register NSAR.
D5	LDI0N	**Low Data Space on ICHN2 Notify:** This bit is used to enable the LDI0 bit in Register NSAR.
D6	NSR1N	**No Status Space on ICHN2 Notify:** This bit is used to enable the NSR1 bit in Register NSAR.
D7	NSR0N	**Low Data Space on ICHN2 Notify:** This bit is used to enable the NSR0 bit in Register NSAR.

Limit Address Register (LAR)

The Limit Address Register (LAR) is used to program the parameters for an LMOP (Limit RAM Operation) service function.

This register is not altered upon reset.

Access Rules

Address	Read	Write
10Ch	Always	Always

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
LRA3	LRA2	LRA1	LRA0	LMRW	RES	RES	LRD8

Bit	Symbol	Description
D0	LRD8	**Limit RAM Data Bit 8:** This bit contains the most-significant data bit read or written from the addressed limit RAM Register. Bits LDR8 and LDR7 are "don't cares" when using small (1 kByte) queues.
D2–D1	RES	**Reserved**
D3	LMRW	**LMOP Read/Write:** This bit determines whether a LMOP service function will be a read (LMRW) = 1) or write (LMRW = 0).
D4–D7	LRA3–LRA0	**Limit RAM Register Address:** Used to program the Limit RAM Register address for a subsequent LMOP service function.

7.0 Control Information (Continued)

Limit Data Register (LDR)

The Limit Data Register (LDR) is used to hold the 8 least-significant Limit RAM data bits transferred in an LMOP service function. (The most-significant data bit is in the Limit Address Register.)

This register is not altered upon reset.

Access Rules

Address	Read	Write
10Dh	Always	Always

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
LRD7	LRD6	LRD5	LRD4	LRD3	LRD2	LRD1	LRD0

Bit	Symbol	Description
D7–D0	LRD7–0	**Limit RAM Data Bit 7–0:** This bit contains the least-significant data bit read or written from or to a Limit RAM Register in an LMOP service function. Bit LDR7 is a "don't care" when using small (1 kByte) queues.

7.0 Control Information (Continued)

Request Attention Register (RAR)

The Request Attention Register (RAR) is used to present exception, breakpoint, request complete, and unserviceable request attentions generated by each Request Channel. Each bit may be enabled by setting the corresponding bit in the Request Notify Register.

All bits in this register are set to Zero upon reset.

Access Rules

Address	Read	Write
10Eh	Always	Conditional

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
USRR0	RCMR0	EXCR0	BRKR0	USRR1	RCMR1	EXCR1	BRKR1

Bit	Symbol	Description
D0	BRKR1	**Breakpoint on RCHN1:** Is set by the MACSI device when a CNF Descriptor is written on RCHN1. No action is taken by the MACSI device if the host sets this bit.
D1	EXCR1	**Exception on RCHN1:** Is set by the MACSI device when an exception occurs on RCHN1. An exception condition consists of one of the following events: ABus Error, Consistency Failure (REQ or ODUD), BMAC MAC Reset, Timeout (TRT expires), BMAC abort (MAC frame received or FC/Request Class inconsistency), RINGOP change, host abort (via SAR register), FIFO underrun, or confirmation exception (for full Confirmation). No action is taken by the MACSI device if the host sets this bit. This bit indicates that a request on RCHN1 did not complete normally. This implies that an exception event occurred or that the Request is improperly formed. The corresponding Confirmation (CNF) Descriptor will give more status about the failure. The additional information in the CNF descriptor should be used to make a decision about the severity of the error. If the exception was caused by an ABus error, the RQSTOP will also be set.
D2	RCMR1	**Request Complete on RCHN1:** Is set by the MACSI device when it has completed processing a Request object on RCHN1. This completion may be a normal completion where a request object was transmitted without error. It may also be an abnormal completion due to one of the exception conditions listed above in EXCR1. No action is taken if the Host sets this bit.
D3	USRR1	**Unserviceable Request on RCHN1:** Is set by the MACSI device when a Request cannot be processed on RCHN1. This occurs when the Request Class is inappropriate for the current ring state (e.g., Asynchronous transmission while RINGOP = 0), or when there is no CNF status space, or when the host aborts a request by clearing the ABR bit in the Service Attention Register. While this bit is set, no requests will be processed on RCHN1. The host must clear this bit to resume request processing. If the USRR1 was set due to lack of CNF space, this condition must be corrected by giving the MACSI device more CNF space before restarting the channel. If it was due to a request class/RINGOP incompatibility, then the reason for the incompatibility must be resolved.
D4	BRKR0	**Breakpoint on RCHN0:** Is set by the MACSI device when a CNF Descriptor is written on RCHN0. No action is taken by the MACSI device if the host sets this bit.

Bit	Symbol	Description
D5	EXCR0	**Exception on RCHN0:** This bit is set by the MACSI device when an exception occurs on RCHN0. An exception condition consists of one of the following events: ABus Error, Consistency Failure (REQ or ODUD), BMAC MAC Reset, Timeout (TRT expires), BMAC abort (MAC frame received or FC/Request Class inconsistency), RINGOP change, host abort (via SAR register), FIFO underrun, or confirmation exception (for full Confirmation). No action is taken by the MACSI device if the host sets this bit. This bit indicates that a request on RCHN0 did not complete normally. This implies that an exception event occurred or that the Request is improperly formed. The corresponding Confirmation (CNF) Descriptor will give more status about the failure. The additional information in the CNF descriptor should be used to make a decision about the severity of the error. If the exception was caused by an ABus error, the RQSTOP will also be set.
D6	RCMR0	**Request Complete on RCHN0:** Is set by the MACSI device when it has completed processing a Request object on RCHN0. This completion may be a normal completion where a request object was transmitted without error. It may also be an abnormal completion due to one of the exception conditions listed above in EXCR0. This bit, (together with the Breakpoint bit BRKR0) indicates that there are CNF descriptors to be processed. No action is taken if the Host sets this bit.
D7	USRR0	**Unserviceable Request on RCHN0:** This bit is set by the MACSI device when a Request cannot be processed on RCHN0. This occurs when the Request Class is inappropriate for the current ring state (e.g., Asynchronous transmission while RINGOP = 0), or when there is no CNF status space, or when the host aborts a request by clearing the ABR bit in the Service Attention Register. While this bit is set, no requests will be processed on RCHN0. The host must clear this bit to resume request processing. If the USRR0 was set due to lack of CNF space, this condition must be corrected by giving the MACSI device more CNF space before restarting the channel. If it was due to a request class/RINGOP incompatibility, then the reason for the incompatibility must be resolved.

7.0 Control Information (Continued)

Request Notify Register (RNR)

The Request Notify Register (RNR) is used to enable attentions in the Request Attention Register (RAR). If a bit in Register RNR is set to One, the corresponding bit in Register RAR will be applied to the Master Attention Register, which can be used to generate an interrupt to the host.

All bits in this register are set to Zero upon reset.

Access Rules

Address	Read	Write
10Fh	Always	Always

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
USRR0N	RCMR0N	EXCR0N	BRKR0	USRR1N	RCMR1N	EXCR1N	BRKR1N

Bit	Symbol	Description
D0	BRKR1N	**Breakpoint on RCHN1 Notify:** This bit is used to enable the BRKR1 bit in Register RAR.
D1	EXCR1N	**Exception on RCHN1 Notify:** This bit is used to enable the EXCR1 bit in Register RAR.
D2	RCMR1N	**Request Complete on RCHN1 Notify:** This bit is used to enable the RCMR1 bit in Register RAR.
D3	USRR1N	**Unserviceable Request on RCHN1 Notify:** This bit is used to enable the USRR1 bit in Register RAR.
D4	BRKR0N	**Breakpoint on RCHN0 Notify:** This bit is used to enable the BRKR0 bit in Register RAR.
D5	EXCR0N	**Exception on RCHN0 Notify:** This bit is used to enable the EXCR0 bit in Register RAR.
D6	RCMR0N	**Request Complete on RCHN0 Notify:** This bit is used to enable the RCMR0 bit in Register RAR.
D7	USRR0N	**Unserviceable Request on RCHN0 Notify:** This bit is used to enable the USRR0 bit in Register RAR.

7.0 Control Information (Continued)

Request Channel 0 and 1 Configuration Registers 0 (R0CR0 and R1CR0)

The two Request Configuration Registers 0 (R0CR0 and R1CR0) are programmed with operational parameters for each of the Request Channels. Additional Request Channel parameters are configured in Request Configuration Registers 1. These registers may only be altered between Requests, i.e., while the particular Request Channel does not have a Request loaded.

These registers are not altered upon reset.

Access Rules

Address	Read	Write
110–111h	Always	Always

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
TT1	TT0	PRE	HLD	FCT	SAT	VST	FCS

Bit	Symbol	Description
D0	FCS	**Frame Check Sequence Disable:** When this bit is set, the MACSI device asserts the FCST signal throughout the request. This drives the Ring Engine FCST signal. This bit is used to program the Ring Engine (MAC) not to concatenate its generated FCS to the transmitted frame. The Valid FCS bit in the Expected Frame Status Register independently determines whether a frame needs a valid FCS to meet the matching frame criteria.
D1	VST	**Void Stripping:** When this bit is set, the MACSI device asserts the STRIP signal out throughout the request. This drives the Ring Engine STRIP (Void Strip) signal. The STRIP signal may also drive the Ring Engine SAT signal, depending on the state of the BOSEL bit. See "MAC Mode Register 2 (MCMR2)".
D2	SAT	**Source Address Transparency:** When this bit is set, the MACSI device asserts the SAT output signal throughout the request. This drives the Ring Engine SAIGT signal. It may optionally drive the SAT signal depending upon the setting of the BOSEL bit. See "MAC Mode Register 2 (MCMR2)". When SAT is set, Full Confirmation requires the use of the EM (External SA Match) signal.
D3	FCT	**Frame Control Transparency:** When this bit is set, the FC will be sourced from the ODU (not the REQ.First or REQ.Only Descriptor). When Full Confirmation is enabled and FCT = 0, all bits of the FC in returning frames must match the FC field in the REQ Descriptor; if FCT = 1, only the C, L and r bits must match. Note that since the MACSI device decodes the REQ.F Descriptor FC field to determine whether to assert RQCLM/RQBCN, FC transparency may be used to send Beacons or Claims in any ring non-operational state, as long as the FC in the REQ Descriptor is not set to Beacon or Claim. By programming a Beacon or Claim FC in the REQ Descriptor, then using FC transparency, any type of frame may be transmitted in the Beacon or Claim state.
D4	HLD	**Hold:** When this bit is set, the MACSI device will not end a service opportunity until the Request is complete. When this bit is Zero, the MACSI device ends the service opportunity on the Request Channel when all of the following conditions are met: 1. There is no valid request active on the Request Channel. 2. The service class is non-immediate. 3. There is no data in the FIFO. 4. There is no valid REQ fetched by the MACSI device. This bit also affects Prestaging on RCHN1 (Request Channel 1). When HLD = 0, prestaging is enabled on RCHN1, regardless of the state of the PRE bit (except for Immediate service classes). When HLD = 1, prestaging is determined by the PRE bit. This option can potentially waste ring bandwidth, but may be required (particularly on RCHN0, Request Channel 0) if a guaranteed service time is required. When using the Repeat option, HLD is required for small frames. If HLD is not used, the other Request Channel will be checked for service before releasing the token between frames. This may not be the desired action, particularly if there is a request on RCHN1 that needs servicing after the completion of RCHN0's Repeated Request.

Bit	Symbol	Description
D5	PRE	**Preempt/Prestage:** When this bit is set, preemption is enabled for RCHN0, and prestaging is enabled for RCHN1 (prestaging is always enabled for RCHN0). When this bit is Zero, preemption is disabled and Prestaging is enabled on the RCHN0. When preemption is enabled, RCHN0 preempts a (non-committed) frame of RCHN1 already in the FIFO, causing it to be purged and refetched after RCHN0's request has been serviced. When the Request Machine servicing on RCHN1 and a request on RCHN0 becomes active, if preemption is enabled on RCHN0, the Request Machine will finish transmitting the current frame on RCHN1, then release the token and move back to the start state. This has the effect of reprioritization of the Request Channels, thus ensuring that frames on RCHN0 are transmitted at the next service opportunity. When RCHN0 has been serviced, transmission will continue on RCHN1 with no loss of data. When prestaging is enabled, the next frame for RCHN1 is staged (ODUs are loaded into the FIFO before the token arrives). If prestaging is not enabled, the Request Machine waits until the token is captured before staging the first frame. Once the token is captured, the Request Machine begins fetching data, and when the FIFO threshold has been reached, transmits the data on the Request Channel. For requests with an Immediate service class, prestaging is not applicable. When this bit is Zero, preemption is disabled for RCHN0, and request on RCHN1 will not be prestaged unless the HLD bit is Zero, in which case RCHN1 will prestage data regardless of the setting of the PRE bit. Note that when prestaging is not enabled on RCHN1, data is not staged until the token is captured. Since there is no data in the FIFO (if there is no active request on RCHN0), the MACSI device will immediately release the token if the HLD option is not set.
D7–D6	TT1–0	**Transmit Threshold:** These bits in conjunction with the EFT bit, determine the threshold on the output data FIFO before the MACSI device requests transmission. See "Request Channel 0 and 1 Configuration Registers 1 (R0CR1 and R1CR1)". **TT1** **TT0** **Threshold Value** 0 0 8 Words or 512 Words 0 1 16 Words or Reserved 1 0 128 Words or Reserved 1 1 256 Words or End of Frame

Request Channel 0 and 1 Expected Frame Status Registers (R0EFSR and R1EFSR)

The Expected Frame Status Registers (R0EFSR and R1EFSR) define the matching criteria used for Full Confirmation of returning frames on each Request Channel. A returning frame must meet the programmed criteria to be counted as a matching returning frame on each Request Channel. A returning frame must meet the programmed criteria to be counted as a matching returning frame.

These registers are not altered upon reset.

Access Rules

Address	Read	Write
112–113h	Always	Always

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
VDL	VFCS	EE1	EE0	EA1	EA0	EC1	EC0

Bit	Symbol	Description
D1–D0	EC1–0	**Expected C Indicator:** **EC1 EC0 Value** 0 0 Any 0 1 R 1 0 S 1 1 R or S
D3–D2	EA1–0	**Expected A Indicator:** **EA1 EA0 Value** 0 0 Any 0 1 R 1 0 S 1 1 R or S
D5–D4	EE1–0	**Expected E Indicator:** **EE1 EE0 Value** 0 0 Any 0 1 R 1 0 S 1 1 R or S
D6	VFCS	**Valid FCS:** When this bit is set, returning frames must have a valid FCS field to meet the confirmation criteria.
D7	VDL	**Valid Data Length:** When this bit is set, returning frames must have a valid VDL field to meet the confirmation criteria.

7.0 Control Information (Continued)

Indicate Attention Register (IAR)

The Indicate Attention Register (IAR) is used to present exception and breakpoint attentions generated by each Indicate Channel. An Attention bit is set by hardware when an exception or breakpoint occurs on the corresponding Indicate Channel.

Each bit may be enabled by setting the corresponding bit in the Indicate Notify Register.

All bits in this register are set to Zero upon reset.

Access Rules

Address	Read	Write
114h	Always	Conditional

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
RES	RES	EXCI0	BRKI0	EXCI1	BRKI1	EXCI2	BRKI2

Bit	Symbol	Description
D0	BRKI2	**Breakpoint on ICHN2:** This bit is set when a breakpoint is detected on Indicate Channel 2. No action is taken if the host sets this bit.
D1	EXCI2	**Exception on ICHN2:** While this bit is set, copying is disabled on ICHN2. This bit is set by the MACSI device when an exception occurs on Indicate Channel 2. An exception consists of an ABus error during an IDU or IDUD write for ICNH2. It may be set by the host to disable copying on ICHN2, which is convenient when updating the Indicate Header Length and Indicate Threshold register. When this bit is set by the device it signifies that the last frame received on this channel had an ABus error. It is the last frame because the setting of this bit disables further copying on this channel. The last frame should be discarded.
D2	BRKI1	**Breakpoint on ICHN1:** This bit is set when a breakpoint is detected on Indicate Channel 1. No action is taken if the host sets this bit.
D3	EXCI1	**Exception on ICHN1:** While this bit is set, copying is disabled on ICHN1. This bit is set by the MACSI device when an exception occurs on Indicate Channel 1. An exception consists of an ABus error during an IDU or IDUD write for ICNH1. It may be set by the host to disable copying on ICHN1, which is convenient when updating the Indicate Header Length and Indicate Threshold register. When this bit is set by the device it signifies that the last frame received on this channel had an ABus error. It is the last frame because the setting of this bit disables further copying on this channel. The last frame should be discarded.
D4	BRKI0	**Breakpoint on ICHN0:** This bit is set when a breakpoint is detected on ICHN0. No action is taken if the host sets this bit.
D5	EXCI0	**Exception on ICHN0:** While this bit is set, copying is disabled on ICHN0. This bit is set by the MACSI device when an exception occurs on Indicate Channel 0. An exception consists of an ABus error during an IDU or IDUD write for ICNH0. It may be set by the host to disable copying on ICHN0. When this bit is set by the device it signifies that the last frame received on this channel had an ABus error. It is the last frame because the setting of this bit disables further copying on this channel. The last frame should be discarded.
D7–D6	RES	**Reserved**

7.0 Control Information (Continued)

Indicate Notify Register (INR)

The Indicate Notify Register (INR) is used to enable attentions in the Indicate Attention Register (IAR). If a bit in Register INR is set to One, the corresponding bit in Register IAR will be applied to the Master Attention Register, which can be used to generate an interrupt to the host.

All bits in this register are set to Zero upon reset.

Access Rules

Address	Read	Write
115h	Always	Always

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
RES	RES	EXC0N	BRK0N	EXC1N	BRK1N	EXC2N	BRK2N

Bit	Symbol	Description
D0	BRK2N	**Breakpoint on ICHN2 Notify:** This bit is used to enable the BRK2 bit in Register IAR.
D1	EXC2N	**Exception on ICHN2 Notify:** This bit is used to enable the EXC2 bit in Register IAR.
D2	BRK1N	**Breakpoint on ICHN1 Notify:** This bit is used to enable the BRK1 bit in Register IAR.
D3	EXC1N	**Exception on ICHN1 Notify:** This bit is used to enable the EXC1 bit in Register IAR.
D4	BRK0N	**Breakpoint on ICHN0 Notify:** This bit is used to enable the BRK0 bit in Register IAR.
D5	EXC0N	**Exception on ICHN0 Notify:** This bit is used to enable the EXC0 bit in Register IAR.
D7–D6	RES	**Reserved**

Indicate Threshold Register (ITR)

The Indicate Threshold Register (ITR) specifies the maximum number of frames that can be received on Indicate Channel 1 or Indicate Channel 2 before an attention will be generated. This register may be written only when the INSTOP bit in the State Attention Register is set, or when the Indicate Channel's corresponding EXC bit in the Indicate Attention Register is set.

This register is not altered upon reset.

Access Rules

Address	Read	Write
116h	Always	INSTOP Mode or EXC = 1 Only

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
THR7	THR6	THR5	THR4	THR3	THR2	THR1	THR0

Bit	Symbol	Description
D7–D0	THR7–0	**Threshold Data Bits 7–0:** The value programmed in this register is loaded into an internal counter every time the Indicate Channel changes. Each valid frame copied on the current Channel decrements the counter. When the counter reaches Zero, a status breakpoint attention is generated (i.e., the Channel's BRK bit in the Indicate Attention Register is set) if the Channel's Breakpoint on Threshold (BOT) bit in the Indicate Mode Register is set. Loading the Indicate Threshold Register with Zero generates a breakpoint after 256 consecutive frames are received on any one Indicate Channel.

7.0 Control Information (Continued)

Indicate Mode Configuration Register (IMR)

The Indicate Mode Configuration Register (IMCR) defines configuration options for all three indicate Channels, including the sort mode, frame filtering, and status breakpoints.

This register may be written only when the INSTOP bit in the State Attention Register is set. It may be written with its current value any time, which is useful for one-shot sampling.

This register is not altered upon reset.

Access Rules

Address	Read	Write
117h	Always	INSTOP Mode Only

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
SM1	SM0	SKIP	FPP	BOT2	BOT1	BOB	BOS

Bit	Symbol	Description
D0	BOS	**Breakpoint on Service Opportunity:** Enables the end of a service opportunity to generate an Indicate breakpoint attention (i.e., set the Channel's BRK bit in the Indicate Attention Register). Service opportunities include receipt of a Token, a MAC Frame, or a ring operational change following some copied frames. This bit should be set to 1 if BRKI0 will be used.
D1	BOB	**Breakpoint on Burst:** Enables the end of a burst to generate an Indicate breakpoint attention (i.e., set the Channel's BRK bit in the Indicate Attention Register). End of burst includes Channel change, DA change, SA change, or MAC INFO change. A Channel change is detected from the FC field of valid, copied frames. A DA change is detected when a frame's DA field changes from this station's address to any other. An SA change is detected when a frame's SA field is not the same as the previous one. A MAC INFO change occurs when a MAC frame does not have the identical first four bytes of INFO as the previous frame. This breakpoint always sets the BRK bit (i.e., this breakpoint is always enabled).
D2	BOT1	**Breakpoint on Threshold for ICHN1:** Enables the value in the Indicate Threshold Register to be used to generate an Indicate breakpoint attention on Indicate Channel 1 (i.e., set the BRK1 bit in the Indicate Attention Register).
D3	BOT2	**Breakpoint on Threshold for ICHN2:** Enables the value in the Indicate Threshold Register to be used to generate an Indicate breakpoint attention on Indicate Channel 2 (i.e., set the BRK2 bit in the Indicate Attention Register).
D4	FPP	**Frame-per-Page:** This bit controls how received frames are packed into the Pool Space Pages which are provided via the PSP Descriptors. When this bit is reset, the MACSI device assembles multiple frames into a single page of Pool Space when possible (i.e., the frames are smaller than the 4 kByte page size). When this bit is set, the MACSI device will force a page break and fetch a new PSP for each frame received. This guarantees that no page will contain more than one frame. When FPP is set, Frame packing can be re-enabled on individual channels. See "Address Configuration Register (ACR)". This mode is useful for systems where received frames are not processed in order of receipt. This is because space reclamation is greatly simplified. A side affect of this mode is that no frame will span more than two pages (i.e., a frame will have at most two IDUDs).
D5	SKIP	**Skip Enable:** Enables filtering on Indicate Channel 0 when the Copy Control field for ICHN0 in the Indicate Configuration Register is set to 01 or 10. When this bit is set, only the unique MAC frames received on Indicate Channel 0 will be copied to memory (i.e., those having an FC field or first four bytes of the Information field that differs from the previous frame). When this bit is 0, no MAC frames will be copied. When this bit is changed from a 1 to a 0, the next MAC frame is copied, even if it is the same as the previous frame. A write to the Indicate Mode Register during normal operation disables filtering.

Bit	Symbol	Description
D7–D6	SM1–0	**Sort Mode:** These bits determine how the MACSI device sorts Indicate data onto Indicate Channels 1 and 2.

SM1	SM0	ICHN2	ICHN1
0	0	Asynchronous	Synchronous
0	1	External	Internal
1	0	Info	Header
1	1	Low Priority	High Priority

The Synchronous/Asynchronous Sort Mode is intended for use in end-stations or applications using synchronous transmission.

The Internal/External Sorting Mode is intended for bridging or monitoring applications. MAC/SMT frames matching the internal Ring Engine (MAC) address are sorted onto ICHN0, and all other frames matching the Ring Engine's internal address (short or long) are sorted onto ICHN1. All frames matching the external address (frames requiring bridging) are sorted onto ICHN2. This sorting mode uses the EM, ECOPY, and ECIP input signals with external address matching circuitry. See the section on External address matching for a full description of the timing required on these signals (Section 6.3). Promiscuous mode on ICHN2 does not require any external matching logic to copy frames.

The Header/Info Sort Mode is intended for high performance protocol processing. MAC/SMT frames are sorted onto ICHN0, while all other frames are sorted onto ICHN1 and ICHN2. Frame bytes from the FC up to the programmed header length are copied onto ICHN1. The remaining bytes(info) are copied onto ICHN2. Only one stream of IDUDs is produced (on ICHN1), but both Indicate Channel's PSP queues are used for space (i.e., PSPs from ICHN1 for header space, and PSPs from ICHN2 for info space). Frames may comprise a header only, or a header + info. For frames with info, multi-part IDUD objects are produced. For multi-part IDUDs, the Indicate Status field in the IDUD is used to determine which part of the IDUD object points to the end of the header. The remainder of the IDUD is used to determine which part of the IDUD object points to the end of the header. The remainder of the IDUD object points to the Info. If Pool Space is only declared for ICNH1, then only the Headers will be written to memory. This is useful for protocol monitor applications.

For example, if page crosses occur while writing the header and while writing out the Info, the MACSI device will generate a four part IDUD object (IDUD.First, IDUD.Middle, IDUD.Middle, IDUD.Last). The IDUD.First will have a status of "page cross". The first IDUD. Middle will have a status of "end of header". The next IDUD.Middle will have a status of "page cross". The IDUD.Last will have an "end of frame" status.

The High Priority/Low Priority Sort Mode is intended for end stations using two priority levels of asynchronous transmission. The priority is determined by the most-significant z-bit of the FC (zzz = 0xx = low-priority; zzz = 1xx = high priority). Synchronous frames are sorted onto ICHN1 and MAC/SMT frames are sorted onto ICHN0.

7.0 Control Information (Continued)

Indicate Copy Configuration Register (ICCR)

The Indicate Copy Configuration Register (ICCR) is used to program the copy criteria for each of the Indicate Channels. This register is not altered upon reset.

Access Rules

Address	Read	Write
118h	Always	Always

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
CC0		RES	CC1		RES	CC2	

Bit	Symbol	Description
D1–D0	CC2	**Copy Control ICHN2:** **D1 D0 Copy Mode** 0 0 Do Not Copy 0 1 Copy if (AFLAG | (~ECIP & ECOPY)) & ~MFLAG 1 0 Copy if (AFLAG | (~ECIP & ECOPY)) 1 1 Copy Promiscuously
D2	RES	**Reserved**
D4–D3	CC1	**Copy Control ICHN1:** **D4 D3 Copy Mode** 0 0 Do Not Copy 0 1 Copy if (AFLAG | (~ECIP & ECOPY)) & ~MFLAG 1 0 Copy if (AFLAG | (~ECIP & ECOPY)) 1 1 Copy Promiscuously
D5	RES	**Reserved**
D7–D6	CC0	**Copy Control ICHN0:** **D7 D6 Copy Mode** 0 0 Do Not Copy 0 1 Copy if (AFLAG | (~ECIP & ECOPY)) & ~MFLAG 1 0 Copy if (AFLAG | (~ECIP & ECOPY)) 1 1 Copy Promiscuously

7.0 Control Information (Continued)

Indicate Header Length Register (IHLR)

The Indicate Header Length Register (IHLR) defines the length (in words) of the frame header, for use with the Header/Info Sort Mode.

The Indicate Header Length Register must be initialized before setting the Sort Mode in Header/Info. This register may be changed while the INSTOP bit in the State Attention Register or the EXC bit in the Indicate Attention Register is set.

This register is not altered upon reset.

Access Rules

Address	Read	Write
119h	Always	INSTOP Mode or EXC = 1 Only

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
HL7	HL6	HL5	HL4	HL3	HL2	HL1	HL0

Bit	Symbol	Description
D7–D0	HL7–0	**Header Length:** Specifies the length (in words) of the frame header, for use with the Header/Info Sort Mode. The frame FC is written as a separate word, and thus counts as one word. For example, to split after eight bytes of FDDI INFO in a frame with long addresses, this register is programmed with the value 06 (1 word FC, 1.5 DA, 1.5 SA, 2HDR_DATA). IHLR must not be loaded with a value less than 4. If it is, the MACSI device sets the Command Error (CMDE) and Indicate Stop (INSTOP) attentions. This Register only affects the Header/Info sort mode.

Address Configuration Register (ACR)

This register contains bits for configuring the address swapping logic.

All bits in this register are set to Zero upon reset.

Access Rules

Address	Read	Write
11Ah	Always	Always

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
PCKI2	PCKI1	PCKI0	RSWP1	RSWP0	ISWP2	ISWP1	ISWP0

Bit	Symbol	Description
D0	ISWP0	**Indicate Swap 0:** This bit controls the address swapping logic for Indicate Channel 0 (ICHN0). If this bit is reset, no address swapping takes place. If this bit is set, both Destination (DA) and Source address (SA) fields are swapped from FDDI bit ordering to canonical bit ordering. This involves a bit reversal within each byte.
D1	ISWP1	**Indicate Swap 1:** This bit controls the address swapping logic for Indicate Channel 1 (ICHN1). If this bit is reset, no address swapping takes place. If this bit is set, both Destination (DA) and Source address (SA) fields are swapped from FDDI bit ordering to canonical bit ordering. This involves a bit reversal within each byte.
D2	ISWP2	**Indicate Swap 2:** This bit controls the address swapping logic for Indicate Channel 2 (ICHN2). If this bit is reset, no address swapping takes place. If this bit is set, both Destination (DA) and Source address (SA) fields are swapped from FDDI bit ordering to canonical bit ordering. This involves a bit reversal within each byte.
D3	RSWP0	**Request Swap 0:** This bit controls the address swapping logic for Request Channel 0 (RCHN0). If this bit is reset, no address swapping takes place. If this bit is set, both Destination (DA) and Source address (SA) fields are swapped from canonical bit ordering to FDDI bit ordering. This involves a bit reversal within each byte.
D4	RSWP1	**Request Swap 1:** This bit controls the address swapping logic for Request Channel 1 (RCHN1). If this bit is reset, no address swapping takes place. If this bit is set, both Destination (DA) and Source address (SA) fields are swapped from canonical bit ordering to FDDI bit ordering. This involves a bit reversal within each byte.
D5	PCKI0	**Pack Frames on ICHN0:** This bit controls the packing of Frames into Pool Space Pages for Indicate Channel 0 (ICHN0). When the Frame-Per-Page (FPP) bit is set (see "Indicate Mode Configuration Register (IMR)"), the MACSI device will cause a page break and start each new Frame in a new Pool Space Buffer. Setting the PCKI0 bit selectively disables the Frame-Per-Page mode for ICHN0. If the FPP bit is zero, this PCKI0 bit has no effect.
D6	PCKI1	**Pack Frames on ICHN1:** This bit controls the packing of Frames into Pool Space Pages for Indicate Channel 1 (ICHN1). When the Frame-Per-Page (FPP) bit is set (see "Indicate Mode Configuration Register (IMR)"), the MACSI device will cause a page break and start each new Frame in a new Pool Space Buffer. Setting the PCKI1 bit selectively disables the Frame-Per-Page mode for ICHN1. If the FPP bit is zero, this PCKI1 bit has no effect.
D7	PCKI2	**Pack Frames on ICHN2:** This bit controls the packing of Frames into Pool Space Pages for Indicate Channel 2 (ICHN2). When the Frame-Per-Page (FPP) bit is set (see "Indicate Mode Configuration Register (IMR)"), the MACSI device will cause a page break and start each new Frame in a new Pool Space Buffer. Setting the PCKI2 bit selectively disables the Frame-Per-Page mode for ICHN2. If the FPP bit is zero, this PCKI2 bit has no effect.

7.0 Control Information (Continued)

Request Channel 0 and 1 Configuration Registers 1 (R0CR1 and R1CR1)

The two Request Configuration Registers 1 (R0CR1 and R1CR1) are programmed with additional operational parameters for each of the Request Channels. Other Request Channel parameters are configured in Request Configuration Registers 0. These registers may only be altered between Requests, i.e., while the particular Request Channel does not have a Request loaded.

All bits in these registers are set to Zero upon reset.

Access Rules

Address	Read	Write
11B–11Ch	Always	Always

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
EFT	RES	RES	RES	RES	RES	RES	ETR

Bit	Symbol	Description
D0	ETR	**Early Token Request:** When this bit is set, the MACSI device attempts to capture a token as soon as a valid Request Descriptor (REQ) is fetched for this channel. This allows the user to maintain tight control over the Token access timing by pacing REQ availability. This is useful for certain models of Synchronous traffic use. If this bit is reset, the MACSI device will not capture a Token until enough data for this request has been fetched to reach the Transmit Data FIFO threshold or the end-of-frame is fetched into the FIFO. This bit should normally be reset because this will save ring bandwidth.
D6–D1	RES	**Reserved**
D7	EFT	**Extended FIFO Threshold:** This bit is used to extend the number of FIFO thresholds available with the TT[1:0] bits in R0CR0 and R1CR0. See "Request Channel 0 and 1 Configuration Registers 0 (R0CR0 and R1CR0)". The table below shows the thresholds available. The MACSI device Transmit Data FIFO is large enough to hold an entire maximum length FDDI frame. The "End of Frame" threshold is used to tell the MACSI device not to start transmitting until the entire frame has been staged in the FIFO.

EFT	TT[1]	TT[0]	Threshold
0	0	0	8 words
0	0	1	16 words
0	1	0	128 words
0	1	1	256 words
1	0	0	512 words
1	0	1	Reserved
1	1	0	Reserved
1	1	1	End of Frame

System Interface Compare Register (SICMP)

The System Interface Compare Register (SICMP) is used in comparison with a write access of a conditional write register. The System Interface Compare Register is loaded on a read of any of the system interface conditional event Attention Registers or by directly writing to it.

This register is not altered upon reset.

Access Rules

Address	Read	Write
11Fh	Always	Always

Register Bits

D7	D6	D5	D4	D3	D2	D1	D0
CMP7	CMP6	CMP5	CMP4	CMP3	CMP2	CMP1	CMP0

Bit	Symbol	Description
D7–D0	CMP7–CMP0	**Compare:** These bits are compared to bits D7–D0 of the accessed System Interface register. Only the bits in the System Interface Attention Register that have the same current value as the corresponding bit in the Compare register will be updated with the new value.

7.8 POINTER RAM REGISTERS

Pointer RAM Registers contain pointers to all data and Descriptors manipulated by the MACSI device, namely, Input and Output Data Units, Input and Output Data Unit Descriptors, Request Descriptors, Confirmation Messages, and Pool Space Descriptors. Pointer RAM Registers are shown in *Figure 7-3.*

7.9 LIMIT RAM REGISTERS

The Limit RAM Registers are used by both the Indicate and Request machines. Limit RAM Registers contain data values that define how far the MACSI device may advance in each of its ten queues. The Limit RAM Registers do **not** define the wrap point for each queue which is fixed at either 1 kByte or 4 kBytes. Limit RAM Registers are shown in *Figure 7-4.*

7.10 DESCRIPTORS

Descriptors are used to observe and control the operation of the MACSI device. They contain address, status, and control information about Indicate and Request operations. Descriptors are stored in lists and wrap-around queues in memory external to the MACSI device and accessed by the MACSI device via the ABus. Descriptors include the following: Input Data Unit Descriptors (IDUDs) specify the location, size, part, and status information for Input Data Units. Output Data Unit Descriptors (ODUDs) specify the location and size of Output Data Units. For multi-ODUD frames, they also specify which part of the frame is pointed to by the ODUD. Pool Space Descriptors (PSPs) describe the location and size of a region of memory space available for writing Indicate data. Request Descriptors (REQs) describe the location of a stream of Output Data Unit Descriptors and contain operational parameters. Confirmation Status Messages (CNFs) describe the result of a Request operation.

7.11 OPERATING RULES

Multi-Byte Register Ordering

When referring to multi-byte fields, byte 0 is always the most significant byte. When referring to bits within a byte, bit 7 is the most significant bit and bit 0 is the least significant bit. When referring to the contents of a byte, the most significant bit is always referred to first.

7.0 Control Information (Continued)

7.12 POINTER RAM REGISTER DESCRIPTIONS

The Pointer RAM Register set contains 32, 28-bit registers. Registers 23 through 31 are reserved, and user access of these locations produces undefined results. Pointer RAM Registers are read and written by the host using the Pointer RAM Operation (PTOP) service function and are accessed directly by MACSI device hardware during Indicate and Request operations. After initialization, the Pointer RAM Registers are maintained by the MACSI device and do not require host intervention.

During Indicate and Request operations, Pointer RAM registers are used as addresses for ABus accesses of data and Descriptors, i.e., the subchannel addresses for loads (reads) of streams of PSPs, ODUs, ODUDs, and REQs, and for stores (writes) of streams of IDUs, IDUDs, and CNFs.

Pointer RAM Registers include the following:

ODU Pointer: Contains the address of an Output Data Unit. During Request operations, this register is loaded by the MACSI device from the Location Field of its Output Data Unit Descriptor.

ODUD List Pointer: Loaded by the MACSI device from the Location Field of the REQ Descriptor when it is read from memory. The address is incremented by the MACSI device as each ODUD is fetched from memory.

CNF Queue Pointer: Contains the current CNF Status Queue address. This register is written by the user after he has allocated space for the CNF Queue. During Request operations, this register is incremented by the MACSI device after each CNF is written to the CNF Queue.

REQ Queue Pointer: Initialized by the host with the start address of the REQ Descriptor Queue after the Queue has been initialized. During Request operations, the address is incremented by the MACSI device as each REQ is fetched.

IDU Pointer: Written by the MACSI device with the Location Field of the PSP Descriptor when it is loaded from the PSP pre-fetch register.

IDUD Queue Pointer: Points to the Queue location where IDUDs will be stored. Written by the user after he has allocated space for the IDUD Status Queue. Incremented by the MACSI device as IDUDs are written to consecutive locations in the Queue.

PSP Queue Pointer Register: Points to the next available PSP. Initialized by the host with the start address of the PSP Queue. As each PSP is read from memory, this register is incremented.

Next PSP Register: Written by the MACSI device with the PSP fetched from the PSP Queue.

Indicate Shadow Register: Written by the MACSI device with the start address of the last IDU copied to memory.

Request Shadow Register: Written by the MACSI device with the address of the current ODUD.

See *Figure 7-3* for Summary including address and access rules.

7.13 LIMIT RAM REGISTER DESCRIPTIONS

The Limit RAM Register set contains 16, 9-bit registers. Registers 11 through 15 are reserved, and access of these locations produces undefined results.

The Limit RAM registers contain data values that define the limits of each of the ten queues maintained by the MACSI device.

Limit RAM Registers are read and written by the host using the Limit RAM Operation (LMOP) service function when the Status/Space Machine is in STOP Mode, and are read directly by MACSI device hardware during Indicate and Request operations.

Limit RAM Registers include the following:

REQ Queue Limit: Defines the last valid REQ written by the host.

CNF Queue Limit Register: Defines the last Queue location where a CNF may be written by the MACSI device. Due to pipelining, the MACSI device may write up to two CNFs after it detects a write to the next-to-last CNF entry (and generates a No Status Space Attention). For this reason, the host must always define the CNF queue limit to be one Descriptor less than the available space.

IDUD Queue Limit Register: Defines the last Queue location where an IDUD may be written by the MACSI device.

PSP Queue Limit: Defines the last valid PSP written by the host.

See *Figure 7-4* for Summary including address and access rules.

Group	Address	Register Name	Access Rules Read	Write
POINTER RAM	00	ODU Pointer RCHN1 (OPR1)	Always	Always
	01	ODUD List Pointer RCHN1 (OLPR1)	Always	Always
	02	CNF Queue Pointer RCHN1 (CQPR1)	Always	Always
	03	REQ Queue Pointer RCHN1 (RQPR1)	Always	Always
	04	ODU Pointer RCHN0 (OPR0)	Always	Always
	05	ODUD List Pointer RCHN0 (OLPR0)	Always	Always
	06	CNF Queue Pointer RCHN0 (CQPR0)	Always	Always
	07	REQ Queue Pointer RCHN0 (RQPR0)	Always	Always
	08	IDU Pointer ICHN2 (IPI2)	Always	Always
	09	IDUD Queue Pointer ICHN2 (IQPI2)	Always	Always
	0A	PSP Queue Pointer ICHN2 (PQPI2)*	Always	Always
	0B	Next PSP ICHN2 (NPI2)	Always	Always
	0C	IDU Pointer ICHN1 (IPI1)	Always	Always
	0D	IDUD Queue Pointer ICHN1 (IQPI1)	Always	Always
	0E	PSP Queue Pointer ICHN1 (PQPI1)*	Always	Always
	0F	Next PSP ICHN1 (NPI1)	Always	Always
	10	IDU Pointer ICHN0 (IPI0)	Always	Always
	11	IDUD Queue Pointer ICHN0 (IQPI0)	Always	Always
	12	PSP Queue Pointer ICHN0 (PQPI0)*	Always	Always
	13	Next PSP ICHN0 (NPI0)	Always	Always
	14	IDUD Shadow Register (ISR)	Always	Always
	15	ODUD Shadow Register (OSR)	Always	Always
	16–1F	Reserved	N/A	N/A

***Note:** Bit position D2 of these Pointer RAM Locations is always forced to a 1, (The first word of a PSP is not fetched).

FIGURE 7-3. Pointer RAM Registers

Group	Address	Register Name	Access Rules Read	Write
LIMIT RAM	0	REQ Queue Limit RCHN1 (RQLR1)	Always	Always
	1	CNF Queue Limit RCHN1 (CQLR1)	Always	Always
	2	REQ Queue Limit RCHN0 (RQLR0)	Always	Always
	3	CNF Queue Limit RCHN0 (CQLR0)	Always	Always
	4	IDUD Queue Limit ICHN2 (IQLI2)	Always	Always
	5	PSP Queue Limit ICHN2 (PQLI2)	Always	Always
	6	IDUD Queue Limit ICHN1 (IQLI1)	Always	Always
	7	PSP Queue Limit ICHN1 (PQLI1)	Always	Always
	8	IDUD Queue Limit ICHN0 (IQLI0)	Always	Always
	9	PSP Queue Limit ICHN0 (PQLI0)	Always	Always
	A-F	Reserved	N/A	N/A

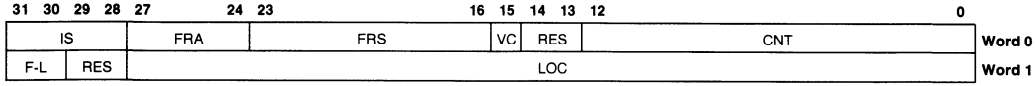
FIGURE 7-4. Limit RAM Registers

Input Data Unit Descriptor (IDUD)

Input Data Unit Descriptors (IDUDs) are generated on Indicate Channels to describe where the MACSI device wrote each frame part and to report status for the frame.

For multi-part IDUDs, intermediate status is written in each IDUD, and when a status event occurs, definitive status is written in the last IDUD.

A detailed description of the encodings of the Indicate Status bits is given in *Figure 7.5.*



Bit	Symbol	Description
Word 0		
D12–D0	CNT	**Byte Count:** Number of bytes in the IDU to which this IDUD points. This count includes the FDDI Frame Check Sequence (4 byte FCS) but it does not include the three FC pad bytes which are written.
D14–D13	RES	**Reserved**
D15	VC	**VCOPY:** Reflects the state of the internal VCOPY signal sent to the Ring Engine by the System Interface for this frame. 0: VCOPY was negated 1: VCOPY was asserted
D23–D16	FRS	**Frame Status:** This C, E, and A fields are valid only if the frame ended with an ED.
D17–D16	C	**C Indicator:** 00: none 01: R 10: S 11: T
D19–D18	A	**A Indicator:** 00: none 01: R 10: S 11: T
D21–D20	E	**E Indicator:** 00: none 01: R 10: S 11: T
D22	VFCS	**Valid FCS:** 0: FCS field was invalid 1: FCS field was valid
D23	VDL	**Valid Date Length:** 0: Data length was invalid 1: Data length was valid

7.0 Control Information (Continued)

Bit	Symbol	Description
Word 0 (Continued)		
D27–D24	FRA	**Frame Attributes:** This field gives termination and address information.
D25–D24	TC	**Termination Condition:** 00: Other (e.g., MAC Reset/token). 01: ED 10: Format error. 11: Frame stripped.
D26	AFLAG	**AFLAG:** Reflects the state of the AFLAG input signal, which is sampled by the MACSI device at INFORCVD. 0: External DA match. 1: Internal DA match.
D27	MFLAG	**MFLAG:** Reflects the state of the MFLAG input signal, which is sampled by the MACSI device at INFORCVD. 0: Frame sent by another station. 1: Frame sent by this station.
D31–D28	IS	**Indicate Status:** The values in this field are prioritized, with the highest number having the highest priority. A detailed description of the encodings are given in *Figure 7-5.* **IS3 (D31) IS2 (D30) IS1 (D29) IS0 (D28) Meaning** **Non-end Frame Status** 0 0 0 0 Last IDU of queue, page-cross. 0 0 0 1 Page boundary crossed. 0 0 1 0 End of header. 0 0 1 1 Page-cross with header-end. **Normal-end Frame Status** 0 1 0 0 Intermediate (no breakpoints). 0 1 0 1 Burst boundary. 0 1 1 0 Threshold. 0 1 1 1 Service opportunity. **Copy Abort due to No Space** 1 0 0 0 No data space. 1 0 0 1 No header space. 1 0 1 0 Good header, info not copied. 1 0 1 1 Not enough info space. **Error** 1 1 0 0 FIFO overrun. 1 1 0 1 Bad frame (no VDL or no VFCS). 1 1 1 0 Parity error. 1 1 1 1 Internal error.
Word 1		
D27–D0	LOC	**Location:** 28-bit memory address of the start of an IDU. For the first IDU of a frame, the address is of the fourth FC byte of the burst-aligned frame (i.e., bits [1:0] = 11). For subsequent IDUs, the address is of the first byte of the IDU (i.e, bits [1:0] = 00).
D29–D28	RES	**Reserved**
D31–D30	F-L	**First/Last Tag:** Identifies the IDU object part, i.e., Only, First, Middle, or Last. FL = 10 = First, FL = 00 = Middle, FL = 01 = Last, FL = 11-Only.

NON-END FRAME STATUS	
[0000]	**Last IDUD of Queue, with a Page Cross:** The last available location of the ICHN's IDUD queue was written. Since there was a page cross, there was more data to be written. Since there was no more IDUD space, the remaining data was not written. Note that this code will not be written in an IDUD.Middle, so that a Zero IS field with Zero F-L tags can be used by software as a null descriptor.
[0001]	**Page Cross:** Must be an IDUD.First or IDUD.Middle. This is part of a frame that filled up the remainder of the current page, requiring a new page for remainder of the data.
[0010]	**Header End:** This refers to the last IDU of the header portion of a frame.
[0011]	**Page Cross and Header End:** The occurrence of a page cross and header end.
NORMAL-END FRAME STATUS	
[0100]	**Intermediate:** A frame ended normally, and there was no breakpoint.
[0101]	**Burst Boundary:** A frame ended normally, and there was a breakpoint because a burst boundary was detected.
[0110]	**Threshold:** The copied frame threshold counter was reached when this frame was copied, and the frame ended normally.
[0111]	**Service Opportunity:** This (normal end) frame was preceeded by a token or MACRST, a MAC frame was received, or there was a ring-op change. Any of these events marks a burst boundary.
NO SPACE COPY ABORT	
[1000]	**Insufficient Data Space:** Not all the frame was copied because there was insufficient data space. This code is only written in non-Header/Info Sort Mode.
[1001]	**Insufficient Header Space:** The frame copy was aborted because there was insufficient header space (in Header/Info Sort Mode0.
[1010]	**Successful Header Copy, Frame Info Not Copied:** There was sufficient space to copy the header, but insufficient data space to copy info, or insufficient IDU space (on ICHN2), or both. No info was copied.
[1011]	**No Info Space:** The frame's header was copied. When copying the data, there was insufficient data and/or IDU space.
ERROR	
[1100]	**FIFO Overrun:** The Indicate FIFO had an overrun while copying this frame. This exception is caused when the memory interface does not allow the MACSI device to empty the data FIFO as quickly as it is being filled. This frame should not be processed because data has been lost.
[1101]	**Bad Frame:** This exception is caused when the incoming frame contains an invalid data length (too short or an odd number of symbols), or an invalid Frame Check Sequence (FCS). This implies that the frame was not a valid FDDI frame. Therefore, this frame should not be processed.
[1110]	**Parity Error:** This exception is caused when the MACSI device detects an internal parity error at the System Interface-Ring Engine interface (the MR.FLOW bit must be set to enable parity checking). This implies a data corruption error within the frame. Therefore, this frame should not be processed.
[1111]	**Internal Error:** This exception is caused when the MACSI device detects an internal hardware error (e.g. illegal state machine state), in the receive logic while receiving a frame. This implies that the frame data may have been corrupted. Therefore, this frame should not be processed. In addition, the MACSI device should be reset and reinitialized.

FIGURE 7-5. Indicate Status Field (IS) of IDU Descriptor

REQ Descriptor (REQ)

Request Descriptors (REQs) contain the part, byte address, and size of one or more Output Data Unit Descriptors. They also contain parameters and commands to the MACSI device associated with Request operations.

Multiple REQ Descriptors (parts) may be grouped as one Request Descriptor object by the host software, with the REQ.First defining the parameters for the entire Request object. Also multiple Output Data Unit Descriptors may be grouped contiguously, to be described by a single REQ Descriptor.

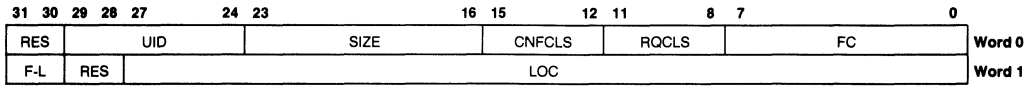
Each REQ part is fetched by the MACSI device from the Request Channel's REQ Descriptor Queue, using the REQ Queue Pointer Register. Each Request Channel processes one Request Object (REQ.Only or REQ.First to REQ.Last set), per service opportunity.

The MACSI device checks for the following inconsistencies when the REQ is loaded from memory:

1. REQ.First with invalid Confirmation Class (as shown in the *Figure 7-7*).
2. REQ.First with Request Class = 0.
3. REQ.First, when the previous REQ was not a REQ.Last or REQ.Only.
4. REQ which is not a REQ.First or REQ.Only when the previous REQ was a REQ.Last or a REQ.Only

When an inconsistency is detected, the MACSI device aborts the Request, and reports the exception in the Request Status field of the CNF Descriptor.

The encodings of the RQCLS and CNFCLS bits are described in more detail in *Figure 7-6* and *Figure 7-7* respectively.



Bit	Symbol	Description
Word 0		
D7–D0	FC	**Frame Control:** This specifies the Frame control field to be used unless FC transparency is enabled. This field is decoded to determine whether to assert RQCLM or RQBCN. This decoding is always active, i.e., regardless of frame control transparency. This field is also used for comparing received frames when confirming (without FC transparency).
D8–D11	RQCLS	**Request/Release Class:** This field encodes the Request Class for the entire Request object, and is thus only sampled on a REQ.First or REQ.Only. The field is asserted on the RQRCLS signals to the Ring Engine when requesting a token. If the Request Class is incompatible with the current ring state, the MACSI device sets the RCHN's USR bit in the Request Attention Register. The encoding of this field is shown in *Figure 7-6*.
D15–D12	CNFCLS	**Confirmation Class:** This field encodes the Confirmation Class for the entire Request object, and is only sampled on a REQ.First or REQ.Only. The encoding of this field is shown in *Figure 7-7*.
D12	E	**End:** Enables confirmation on completion of request. 0: CNFs on completion disabled. 1: CNFs on completion enabled.
D13	I	**Intermediate:** Enables Intermediate (at the end of each Service Opportunity) Confirmation. 0: Intermediate CNFs disabled. 1: Intermediate CNFs enabled.
D14	F	**Full/Transmitter:** Selects between Transmitter and Full Confirmation. 0: Transmitter confirm. 1: Full confirm.

Bit	Symbol	Description
Word 0 (Continued)		
D15–D12	CNFCLS	**Confirmation Class:** (Continued)
D15	R	**Repeat:** Enables repeated transmission of the first frame of the request until the request is aborted. This may be used when sending Beacon or Claim frames. 0: Fetch all frames of REQ. 1: Repeat transmission of first frame of REQ. A Request may use Repeat on RCHN1, and have a Request loaded on RCHN0, but not vice-versa. Specifically, when a Request with the Repeat option is loaded on RCHN0, RCHN1 must not have any REQs active or visible to the MACSI device. Thus REQs on RCHN1 may be queued externally but the queue's Limit Register must not be set at or after that point. Requests with the Repeat option should only be used on one Request Channel at a time, and preferably on RCHN0. Note that the Repeat Option requires a REQ.First Descriptor. The Repeat Option will not work on a REQ.Only Descriptor.
D23–D16	SIZE	**Size:** Count of number of frames represented by the ODUD stream pointed to by REQ.LOC field. Descriptors with a null frame count are permitted, and are typically used to end a Request, without having to send data. For example, to end a restricted dialogue, a REQ.Last with SIZE = 0 will cause the Request Machine to command the Ring Engine to capture and release the specified classes of token. The response of the MACSI device to REQs with SIZE = 0 is as follows: 1. REQ.First: MACSI device latches the REQ Descriptor fields, then fetches the next REQ. RQRCLS is asserted, but RQRDY remains deasserted. 2. REQ.Middle: MACSI device fetches the next REQ. 3. REQ.Only: MACSI device requests the capture of the appropriate token. When it is captured, the MACSI device asserts RQFINAL and ends the request. 4. REQ.Last: MACSI device captures the token, asserts RQFINAL, then marks the request complete.
D29–D24	UID	**User Identification:** Contains the UID field from the current REQ.First or REQ.Only.
D31–D30	RES	**Reserved**
Word 1		
D27–D0	LOC	**Location:** Bits [27:2] are the memory word address of the ODUD stream. Bits [1:0] are expected to be 00, and are not checked.
D29–D28	RES	**Reserved**
D31–D30	F-L	**First/Last Tag:** Identifies the REQ stream part, i.e., Only, First, Middle, or Last. FL = 10 = First, FL = 00 = Middle, FL = 01 = Last, FL = 11-Only.

RQCLS Value	RQCLS Name	Class Type	THT	Token Capture	Token Issue	Notes
0000	None	None		none	none	
0001	Apr1	Async pri1	E	non-r	non-r	
0010	Reserved	Reserved				
0011	Reserved	Reserved				
0100	Syn	Sync	D	any	capt	1
0101	Imm	Immed	D	none	none	4
0110	ImmN	Immed	D	none	non-r	4
0111	ImmR	Immed	D	none	restr	4
1000	Asyn	Async	E	non-r	non-r	
1001	Rbeg	Restricted	E	non-r	restr	2, 3
1010	Rend	Restricted	E	restr	non-r	2
1011	Rcnt	Restricted	E	restr	restr	2
1100	AsynD	Async	D	non-r	non-r	
1101	RbegD	Restricted	D	non-r	restr	2, 3
1110	RendD	Restricted	D	restr	non-r	2
1111	RcntD	Restricted	D	restr	restr	2

E = enabled, D = disabled, non-r = non-restricted, restr = restricted, capt = captured

Note 1: Synchronous Requests are not serviced when bit BCNR of the Ring Event Latch Register is set.

Note 2: Restricted Requests are not serviced when bit BCNR, CLMR, or OTRMAC of the Ring Event Latch Register is set.

Note 3: Restricted Dialogues only begin when a Non-Restricted token has been received and transmitted.

Note 4: Immediate Requests are serviced when the ring is Non-Operational. These requests are serviced from the Data state unless the Request contains a Beacon or Claim FC. If a Claim FC is used, Immediate Requests are serviced from the Claim State. If a Beacon FC is used, Immediate Request are serviced from the Beacon State.

FIGURE 7-6. REQ Descriptor Request Class Encoding

[R]	[F]	[I]	[E]	Confirmation Class
x	0	0	0	Invalid (consistency failure)
x	x	1	0	Invalid (consistency failure)
0	1	0	0	None: Confirmation only on exception
0	0	0	1	Trend: Transmitter confirm, CNF on exception or completion
0	0	1	1	Tint: Transmitter confirm, CNF on exception, completion, or intermediate
0	1	0	1	Fend: Full Confirm, CNF on exception or completion
0	1	1	1	Fint: Full Confirm, CNF on exception, completion, or intermediate
1	1	0	0	NoneR: Confirmation only on exception, repeat frame
1	0	0	1	TendR: Transmitter confirm, CNF on exception or completion, repeat frame
1	0	1	1	TintR: Transmitter confirm, CNF on exception, completion, or intermediate, repeat frame
1	1	0	1	FendR: Full confirmation, CNF on exception or completion, repeat frame
1	1	1	1	FintR: Full Confirmation, CNF on exception, completion, or intermediate, repeat frame

FIGURE 7-7. REQ Descriptor Confirmation Class Field Encodings

Output Data Unit Descriptor (ODUD)

An Output Data Unit Descriptor (ODUD) contains the part, byte address and size of an Output Data Unit. During Request operations, ODUDs are fetched by the MACSI device from a list in memory, using the address in the ODUD List Pointer Register (in the Pointer RAM).

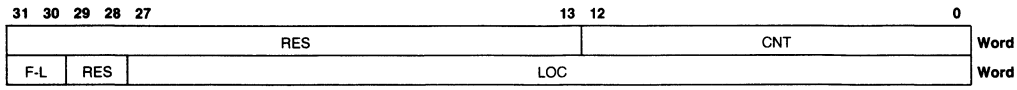
ODUD.Firsts and ODUD.Middles may have a zero byte count, which is useful for fixed protocol stacks. One layer may be called, and if it has no data to add to the frame, it may add an ODUD with a zero byte count to the list. ODUD.Onlys and ODUD.Lasts may not have a zero byte count.

The MACSI device checks for the following inconsistencies when an ODUD is loaded from memory:

1. ODUD.First, when previous ODUD was not an ODUD.Last or ODUD.Only.
2. ODUD which is not an ODUD.First, when the previous ODUD was ODUD.Last or ODUD.Only.
3. ODUD.Last or ODUD.Only with a zero byte count.

When an inconsistency is detected, the MACSI device aborts the Request, and reports the exception in the Request Status field of the CNF Descriptor.

The entire ODUD object must contain at least 4 bytes (for short addresses).



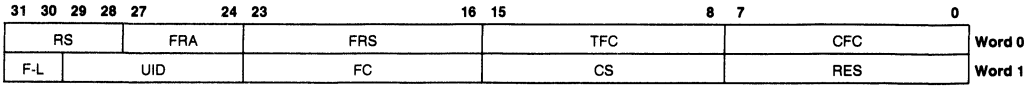
Bit	Symbol	Description
Word 0		
D12–D0	CNT	**Byte Count:** Number of bytes in the ODU. For an ODUD.First or ODUD.Middle the size may be Zero, which is useful for fixed protocol stacks.
D31–D13	RES	**Reserved**
Word 1		
D27–D0	LOC	**Location:** Pointer to the first byte of the corresponding ODU.
D29–D28	RES	**Reserved**
D31–D30	F-L	**First/Last Tag:** Identifies the Output Data Unit part, i.e., Only, First, Middle, or Last. FL = 10 = First, FL = 00 = Middle, FL = 01 = Last, FL = 11-Only.

7.0 Control Information (Continued)

Confirmation Status Message Descriptor (CNF)

A Confirmation Status Message (CNF) describes the result of a Request operation.

A more detailed description of the encoding of the RS bits is given in *Figure 7-8.*



Bit	Symbol	Description
Word 0		
D7–D0	CFC	**Confirmed Frame Count:** Number of confirmed frames. Valid only for Full Confirmation. This count is cumulative for Fint.
D15–D13	TFC	**Transmitted Frame Count:** Number of frames successfully transmitted by the MACSI device. Valid for all confirmation classes. This count is cumulative for Tint and Fint.
D23–D16	FRS	**Frame Status:** This field is valid only for Full Confirmation, and if the frame ended with an ED.
D17–D16	C	**C Indicator:** 00: none 01: R 10: S 11: T
D19–D18	A	**A Indicator:** 00: none 01: R 10: S 11: T
D21–D20	E	**E Indicator:** 00: none 01: R 10: S 11: T
D22	VFCS	**Valid FCS:** 0: FCS field was invalid 1: FCS field was valid
D23	VDL	**Valid Date Length:** 0: Data length was invalid 1: Data length was valid

Bit	Symbol	Description
Word 0 (Continued)		
D27–D24	FRA	**Frame Attributes:** This field is valid only for Full Confirmation.
D25–D24	TC	**Termination Condition:** 00: Other (e.g., MAC Reset/token). 01: ED 10: Format error. 11: Frame stripped.
D26	AFLAG	**AFLAG:** Reflects the state of the AFLAG input signal, which is sampled by the MACSI device at INFORCVD. 0: No DA Match. 1: DA Match.
D27	MFLAG	**MFLAG:** Reflects the state of the MFLAG input signal, which is sampled by the MACSI device at INFORCVD. 0: Frame Sent by another station. 1: Frame Sent by this station.
D31–D28	RS	**Request Status:** This field represents a priority encoded status value, with the highest number having the highest priority. This field is described in *Figure 7-8.*

RS3 D31	RS2 D30	RS1 D29	RS0 D28	Meaning
Intermediate				
0	0	0	0	None
0	0	0	1	Preempted
0	0	1	0	Part Done
Breakpoints				
0	0	1	1	Service Loss
0	1	0	0	Reserved
Completion				
0	1	0	1	Completed Beacon
0	1	1	0	Completed OK
Exception Completion				
0	1	1	1	Bad Confirmation
1	0	0	0	Underrun
1	0	0	1	Host Abort
1	0	1	0	Bad Ringop
1	0	1	1	MAC Abort
1	1	0	0	Timeout
1	1	0	1	MAC Reset
1	1	1	0	Consistency Failure
Error				
1	1	1	1	Internal or Fatal ABus Error

Bit	Symbol	Description
Word 1		
D7–D0	RES	**Reserved**
D15–D8	CS	**Confirmation Status**
D9–D8	FT	**Frame Type:** This field reflects the type of frame that ended Full Confirmation. 00: Any Other. 01: Token. 10: Other Void. 11: My Void.
D10	F	**Full Confirm:** This bit is set when the Request was for Full Conformation.
D11	U	**Unexpected Frame Status:** This bit is set when the frame status does not match the value programmed in the Request Expected Frame Status Register. This applies only to Full Confirmation.
D12	P	**Parity:** This bit is set when a parity error is detected in a received frame. Parity is checked from FC to ED inclusive if the FLOW bit in the Mode Register is set.
D13	E	**Exception:** This bit is part of the MACSI's hierarchical status reporting. It is set when an exception occurs during confirmation. An exception is any one of the nine error or exception codes described in the RS Field. The RCHN's EXC bit in the Request Attention Register is also set.
D14	R	**Ring-Op:** This bit is set when the ring changes operational state after transmission but before all returning frames have been confirmed.
D15	T	**Transmit Class:** 0: Restricted. 1: Non-Restricted.
D23–D16	FC	**Frame Control:** Frame Control field of the last frame of the last confirmed burst. Valid only for Full Confirmation.
D29–D24	UID	**User Identification:** Contains the UID field copied from the current REQ.First or REQ.Only.
D31–D30	F-L	**First/Last Tag:** Identifies the CNF part, i.e., Only, First, Middle, or Last. FL = 10 = First, FL = 00 = Middle, FL = 01 = Last, FL = 11-Only.

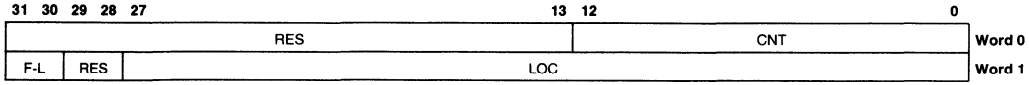
INTERMEDIATE	
[0000]	**NONE:** Non status is written. This may be used by software to identify a NULL or invalid CNF.
[0001]	**Preempted:** RCHN1 was preempted by RCHN0. RCHN1 will be serviced following RCHN0.
[0010]	**Part None:** The MACSI device is servicing a Request, but it cannot hold onto a token, and the last frame of a Request.part has been transmitted.
BREAKPOINTS	
[0011]	**Service Loss:** The THT expired during a Request with THT enabled. Only Occurs for Intermediate Confirmation.
[0100]	**Reserved**
COMPLETION	
[0101]	**Completed Beacon:** When transmitting from the Beacon state, this status is returned when the Ring Engine receives a My_Beacon. When transmitting from the Claim state, this status is returned when the Ring Engine wins the Claim process.
[0110]	**Completed OK:** Normal completion with good status.
EXCEPTION COMPLETION:	In all of the exception and error cases it is likely that at least some of the frames from the associated request were not transmitted properly. Therefore, retransmission may be required. In the case of bad confirmation [0111], the frames may have been transmitted properly but lost on the ring. A consistency failure [1110] means that there is a problem in the request queues. It is recommended that they be reinitialized. The Internal or Abus error code [1111] is very severe and it recommended that the MACSI device be reinitialized.
[0111]	**Bad Confirmation:** This status is reported when there was an error during confirmation. For confirmation, the MACSI device compares the returning frame to the Expected Frame Status (EFS). If these values do not match, the "Bad Confirmation" value is returned in the RS field. If the transmitted frame does not return, (My_Void, Other_Void, or Token received instead) or if the ring state changes, (MAC Reset or the Ring_Operational flag changes), the Bad Confirmation value is also returned.
[1000]	**Underrun:** This exception is caused when the memory interface does not allow the MACSI device to fill the transmit data FIFO as quickly as it is being emptied. It implies that the frame was aborted during transmission.
[1001]	**Host Abort:** This exception is caused when the host software clears the SAR.ABT bit to force an abort or when there is not enough space in the confirmation (CNF) queue. This implies that the Request did not complete normally.
[1010]	**Bad Ringop:** This exception is reported when the Request Class for a Request object is incompatible with the current ring state, (i.e. Immediate class with an operational ring or Async, Sync, or restricted class when the ring state is non-operational). The Request was aborted.
[1011]	**MAC Device Abort:** This exception indicates that the MACSI device aborted the Request and asserted TXABORT. This could be from an interface parity error, or because the transmitted frame failed the FC check, or because the MACSI device received a MAC frame while transmitting in the DATA state. This status is also returned when the MACSI device receives an Other_Beacon while transmitting in the Beacon state, or when the Claim process is lost while transmitting in the Claim state. It implies that the Request did not complete normally.
[1100]	**Timeout:** This exception code indicates that the TRT timer expired during the transmission of a Request with THT disabled. Normally the Ring Engine will finish the current frame and release the Token when the Token Holding Timer (THT) expires. However, for certain requests, the THT can be disabled. In this case, the Token Rotation Timer (TRT) may expire because the station has made the Token Late. The Ring Engine will abort the request and a Timeout will be signaled to the System Interface.
[1101]	**MAC Reset:** This code indicates that the MACSI underwent a MAC Reset during this request. A MAC Reset can be generated by software, (i.e. requested via the control bus), or caused by hardware, (the MACSI state machines entered and illegal state). In either case the Request is aborted.
[1110]	**Consistency Failure:** This code indicates that the MACSI device detected an inconsistency in the REQ or ODUD descriptor queues. For example, if a frame started with on ODUD.First it should be followed by an ODUD.Middle or ODUD.Last. If the next ODUD was another ODUD.First this would be a consistency error. The Request is aborted when a consistency error is detected.
ERROR	
[1111]	**Internal or Fatal ABus Error:** This exception is caused when the MACSI device detects an internal hardware error (e.g. illegal state machine state), in the transmit logic while transmitting a frame. It is also set when an ABus error occurs during frame transmission. It implies that the frame data may not have been transmitted properly.

FIGURE 7-8. Request Status Field (RS) of CNF Descriptor

7.0 Control Information (Continued)

Pool Space Descriptor (PSP)

Pool Space Descriptors (PSPs) contain the address of a free space in host memory available for writing Input Data Units. The count field is not used. The space is assumed to end at the next 4 kByte boundary. When PSPs are read by the MACSI device, the address field of the PSP is loaded into the Indicate Channel's IDU Pointer Register, and is used as the address for the IDU memory write.



Bit	Symbol	Description
Word 0		
D12–D0	CNT	**Byte Count:** Number of bytes of available memory area (this field is currently not used by the MACSI device). To ensure software compatibility with future devices which may use this field, this field may be written with the number of bytes from PSP.LOC to the next 4 kByte boundary.
D31–D13	RES	**Reserved**
Word 1		
D27–D0	LOC	**Location:** Memory byte address of memory area available for writing IDUs. Normally the page offset will be Zero to simplify space management. Must be burst aligned to the size of the largest burst enabled (4 word or 8 word).
D29–D28	RES	**Reserved**
D31–D30	F-L	**First/Last Tag:** Identifies the PSP part, should be PSP.Only (i.e F-L = 11).

8.0 Signal Descriptions

The DP83266 MACSI device is packaged in a 160-pin Plastic Quad Flat Pack. The signals are divided into the following interfaces:

Control Interface: Used for microprocessor access to the Ring Engine and Service Engine.

PHY Interface: Interface signals to the DP83251/55 PLAYER or DP83256/57 PLAYER+.

External Matching Interface: Interface signals used for external address matching.

ABus Interface: Multiplexed Address/Data System Interface.

Electrical Interface: Signals associated with power supply and clocking.

8.1 CONTROL INTERFACE

The Control Interface operates asynchronously to the operation of the data services. During an access, the external Control Bus is synchronized with the internal Control Bus.

The $\overline{ACK}$ and $\overline{INT}$ signals are open drain signals to allow a wired-OR connection of several such signals.

Symbol	Pin #	I/O	Description
CBP	155	I/O	**Control Bus Parity:** Odd parity on CBD7–0.
CBD7–0	154–147	I/O	**Control Bus Data:** Bidirectional Data bus.
CBA8–0	144–136	I	**Control Bus Address:** Address of a particular MACSI device register.
$\overline{CE}$	130	I	**Control Bus Enable:** Handshake signal used to begin a Control Interface access. Active low signal.
R/$\overline{W}$	129	I	**Read/Write:** Determines current direction of a Control Interface access.
$\overline{ACK}$	133	OD	**Acknowledge:** Acknowledges that the Control Interface access has been performed. Active low, open drain signal.
$\overline{INT1-0}$	131, 132	OD	**Interrupt:** Indicates presence of one or more enabled conditions in the Event Registers. One Interrupt signal is provided as an indication to management services and one is provided as an indication to data services. These can be tied together externally to create a single interrupt signal if desired. Active low, open drain signal.

8.0 Signal Descriptions (Continued)

8.2 PHY INTERFACE

The PHY Interface signals transfer symbol pairs between the MACSI and PLAYER+ devices. Transfers are synchronous using the 12.5 MHz Local Byte Clock signal (signal provided by the PLAYER+ device).

A control bit is used to indicate if a Data symbol pair or Control symbol pair or a mixed Control/Data symbol pair are being transferred.

Parity is generated on the PH_Indicate and MA_Indicate data. Parity is checked on the PH_Request and MA_Request data.

Symbol	Pin #	I/O	Description
PRP	122	O	**PHY Request Parity:** Odd parity for PRC and PRD7–0.
PRC	120	O	**PHY Request Control:** 0: Indicates PRD7–0 contains a Data symbol pair. 1: Indicates PRD7–0 contains a Control or mixed Control/Data symbol pair.
PRD7–PRD0	118, 116, 114, 110, 108, 106, 104, 102	O	**PHY Request Data:** Contains a Data or Control symbol pair.
PIP	123	I	**PHY Indicate Parity:** Odd parity for PIC and PID7–0.
PIC	121	I	**PHY Indicate Control:** 0: Indicates PRD7–PRD0 contains a Data symbol pair. 1: Indicates PRD7–PRD0 contains a Control or mixed Control/Data symbol pair.
PID7–PID0	119, 117, 115, 111, 109, 107, 105, 103	I	**PHY Indicate Data:** Contains a Data or a mixed Control/Data symbol pair.

8.0 Signal Descriptions (Continued)

8.2.1 PHY Interface Codes

The DP83256/57 PLAYER+ device converts the Standard 4B/5B FDDI symbol code to the internal code used at the PHY Interface. The PH_DATA.Indication table shows how the Ring Engine interprets the codes generated by the PLAYER+ device and the PH_DATA.Request table shows the codes generated by the Ring Engine.

The internal code is actually an 8B/9B code with parity where one bit is used to determine whether the symbol pair contains two data symbols or at least one control symbol.

PH_DATA.Indication

The Ring Engine interprets the byte stream the PLAYER+ device as defined in Table 8-1.

TABLE 8-1. Internal PHY Indicate Coding

Value	PIP	PIC	PID(7-4)	PID(3-0)	Type
0	1	0	0000	0000	Data Symbol Pair
1	0	0	0000	0001	Data Symbol Pair
:	:	:	:	:	:
254	0	0	1111	1110	Data Symbol Pair
255	1	0	1111	1111	Data Symbol Pair
JK	P	1	1101	xxxx	Start Delimiter
PI	P	1	x011	x1xx	PH_Invalid
PI	P	1	x011	xx1x	PH_Invalid
II	P	1	10xx	xxxx	Idle Symbols
nI	P	1	0000	10xx	Data/Idle Symbol
RR	P	1	0110	0110	Frame Status
RS	P	1	0110	0111	Frame Status
RT	P	1	0110	0101	Frame Status
SS	P	1	0111	0111	Frame Status
SR	P	1	0111	0110	Frame Status
ST	P	1	0111	0101	Frame Status
SX	P	1	0111	xxxx	Frame Status
TX	P	1	0101	xxxx	Ending Delimiter
TR	P	1	0101	0110	Ending Delimiter
TS	P	1	0101	0111	Ending Delimiter
TT	P	1	0101	0101	Ending Delimiter
nT	P	1	0000	0101	Mixed Symbol Pair
Parity Error	$\overline{P}$	0	????	????	Code Violation
Other wise	?	1	Else		Code Violation

where:

PIP PHY Indicate Parity bit, ODD parity

PIC PHY Indicate Control bit:

0 ≥ data byte,

1 ≥ control/mixed byte

PID(7-0) PHY Indicate Data(7-0)

P represents ODD Parity (~$\overline{P}$ is Bad Parity)

x - represents a don't care and is not decoded

? represents a 1 or 0 but not both.

The PLAYER aligns the received JK to a byte boundary. Thus, no provision is made in the internal code or by the Ring Engine for off boundary JKs.

The Idle and PH_Invalid encodings overlap. Idle symbols received while the PLAYER+ device is in Active Line State (ALS) or Idle Line State (ILS0 are not considered PH_INVALID). Idle symbols received while the PLAYER+ device is in states other than ALS or ILS are treated as PH_Invalid.

PH_DATA.Request

The Ring Engine generates the 10-bit byte stream as defined in Table 8-2. Note that all symbol pairs are either control or data symbol pairs. Mixed data/control symbol pairs are never generated or repeated by the Ring Engine.

TABLE 8-2: Internal PHY Request Coding

Value	PRP	PRC	PRD(7-4)	PRD(3-0)	Type
0	1	0	0000	0000	Data Symbol Pair
1	0	0	0000	0001	Data Symbol Pair
:	:	:	:	:	:
254	0	0	1111	1110	Data Symbol Pair
255	1	0	1111	1111	Data Symbol Pair
JK	0	1	1101	1101	Start Delimiter
I I	0	1	1010	1010	Idle Symbols
RR	0	1	0110	0110	Frame Status
RS	1	1	0110	0111	Frame Status
RT	0	1	0110	0101	Frame Status
SS	0	1	0111	0111	Frame Status
SR	1	1	0111	0110	Frame Status
ST	1	1	0111	0101	Frame Status
TR	0	1	0101	0110	Ending Delimiter
TS	1	1	0101	0111	Ending Delimiter
TT	0	1	0101	0101	Ending Delimiter

Where:

PRP — PHY Request Parity bit, parity for all symbol pairs is ODD

PRC — PHY Request control bit:

0 ≥ data byte

1 ≥ control byte

PRD(7-0) PHY Request Data (7-0)

The Ring Engine can repeat the RT and ST symbol pairs but will not generate them.

8.0 Signal Descriptions (Continued)

8.3 EXTERNAL MATCHING INTERFACE

The External Matching Interface provides the means to add external address recognition logic. The results of these address comparisons are conveyed on the appropriate signals.

Symbol	Pin #	I/O	Description
ECIP	86	I	**External Compare In Progress:** This signal is asserted to indicate that external address comparison has begun. It is deasserted to indicate that the comparison has completed. ECOPY and EM are sampled on the rising edge of LBC1 after the deassertion of ECIP. ECIP must be asserted before the seventh byte of the INFO field in order for the MACSI device to recognize an external comparison. It must be deasserted for at least one cycle for the external comparison to complete. If ECIP has not been deasserted before two bytes after the End Delimiter (ED, from the PLAYER+ device), the MACSI device will not copy this frame. ECIP may be implemented as a positive or negative pulse. Note that ECIP will affect the operation of the MACSI device even if the external copy mode is not specifically selected. See section Section 6.3 on page 38 for more details on the external matching interface.
ECOPY	84	I	**External Copy:** Indicates that the current frame should be copied, if possible. Sampled on the rising edge of LBC1 after ECIP is deasserted.
EA	85	I	**External Destination Address Match:** Indicates that an explicit match occurred on the current frame. This affects the setting of the A indicator for this frame. Sampled one byte time before ED is received by the Ring Engine.
EM	87	I	**External Source Address Match:** Indicates that the current frame was transmitted by this station and should be stripped. The Ring Engine will begin stripping three byte times after the assertion of EM. The Service Engine samples EM on the rising edge of LBC1 after the deassertion of ECIP.
LEARN	90	O	**Learn:** Provided for transparent bridging applications. Indicates that the current frame should be copied and the Source Address be added to the address filter database if not already present. This signal is asserted for Long Address frames which were not sourced by this station. If frames are sent using Source Address Transparency (SAT) using the My_Void stripping mechanism, Learn will be false from the transmission of the first SAT frame until after the My_Void frame is received. Learn is valid at the "INFO Received" point for each frame. This is when the fourth byte of INFO field passes between the Ring Engine and the System Interface. This occurs three byte-times after the fourth byte of the INFO field passes between the PLAYER+ device and the MACSI device.

8.0 Signal Descriptions (Continued)

8.4 ABus INTERFACE

The ABus interface signals provide a 28-bit address 32-bit data bus for transfers between the host system and the MACSI device. The ABus uses a bus request/bus grant protocol that allows for multiple bus masters, supports burst transfers of 4 or 8 32-bit words, and permits both physical and virtual addressing using fixed-size pages.

Address and Data:

Symbol	Pin #	I/O	Description
AB__BP3-0	50, 61, 72, 83	I/O	**ABus Byte Parity:** These TRI-STATE signals contain the parity for each address and data byte of AB__AD, such that AB__BP0 is the parity for AB__AD7-0, AB__BP1 is the parity for AB__AD15-8, etc.
AB__AD31-0	40-42, 45-49, 51-53, 56-60, 62-65, 68-71, 73-76, 79-82	I/O	**ABus Address and Data:** These TRI-STATE signals are the multiplexed ABus address and data lines. During the address phase of a cycle, AB__AD27-0 contain the 28-bit address. When SIMR1.EAM = 1, AB__AD31-28 contain a value specified by the user (by programming SIMR1.AB__A31-27) during the address cycle. When SIMR1.EAM = 0, AB__AD31-28 contain a 4-bit function code identifying the type of transaction, encoded as follows: **AB__AD[31:28] — Transaction Type** 0 — RCHN1 ODU Load 1 — RCHN1 ODUD Load/CNF Store 2 — RCHN1 REQ Load 3 — RCHN0 ODU Load 4 — RCHN0 ODUD Load/CNF Store 5 — RCHN0 REQ Load 6 — ICHN2 IDU Store 7 — ICHN2 IDUD Store 8 — ICHN2 PSP Load 9 — ICHN1 IDU Store A — ICHN1 IDUD Store B — ICHN1 PSP Load C — ICHN0 IDU Store D — ICHN0 IDUD Store E — ICHN0 PSP Load F — PTR RAM Load/Store
AB__A27-2	25-19, 16-5, 2-1, 160-156	O	**ABus Demultiplexed Address:** These TRI-STATE signals contain the word address during ABus accesses. They are driven from Tpa to the last Td state, negated in the following Tr state, then released. Note that the timing of these signals is under software control via the System Interface Mode Register 1 (SIMR1). In order for the demultiplexed address bits AB__A27:5 to function properly, SIMR1.ATM must be set to one.

8.0 Signal Descriptions (Continued)

Bus Control:

Symbol	Pin #	I/O	Description
$\overline{AB\_AS}$	39	O	**ABus Address Strobe:** When first asserted, this TRI-STATE signals indicates that address on AB_AD is valid. When this signal is inactive and $\overline{AB\_ACK}$ is asserted, the next cycle is a Recovery State (Tr), in which the bus arbiter can sample all bus requests, then issue a bus grant in the following cycle. Note that the timing of this signal is under software control via Mode Register 1 (MR1).
AB_R/$\overline{W}$	35	O	**ABus Read/Write:** This TRI-STATE signal determines the current direction of an ABus access. A high level indicates a read access and a low level indicates a write access.
$\overline{AB\_DEN}$	34	I/O	**ABus Data Enable:** In normal ABus mode, this TRI-STATE signal indicates that data on AB_AD31–0 is valid. In the enhanced ABus mode for SBus, this signal is an additional Acknowledgment input.
AB_SIZ2–0	31-29	O	**ABus Size:** These TRI-STATE signals indicate the size of the transfer on AB_AD31-0, encoded as follows: **AB_SIZ2 / AB_SIZ1 / AB_SIZ0 / Transfer Size** 0 0 0 — 4 Bytes 0 0 1 — Reserved 0 1 0 — Reserved 0 1 1 — Reserved 1 0 0 — 16 Bytes 1 0 1 — 32 Bytes 1 1 0 — Reserved 1 1 1 — Reserved
$\overline{AB\_ACK}$	37	I	**ABus Acknowledge:** Indicates a bus slave's response to a bus master. The meaning of this signal depends on the state of ABus Error ($\overline{AB\_ERR}$) as well as the ABus mode selected (normal or enhanced). The exact function is described below.
$\overline{AB\_ERR}$	36	I	**ABus Error:** In normal ABus mode, this signal is asserted by a bus slave to cause a transaction retry or transaction abort. In the enhanced ABus mode for SBus, this signal together with $\overline{AB\_ACK}$ and $\overline{AB\_DEN}$ encode the acknowledgment type. The encoding is as follows: **EAM = 0** / **EAM = 1** **$\overline{AB\_ACK}$ / $\overline{AB\_ERR}$ / $\overline{AB\_ACK}$ Ack(2)* / $\overline{AB\_DEN}$ Ack(1)* / $\overline{AB\_ERR}$ Ack(0)* / Function** 1 1 1 1 1 — Wait Cycle 0 1 0 1 1 — Word Acknowledgement 0 0 1 0 0 — Retry 1 0 1 1 0 — Error 0 0 0 — Not Supported 0 0 1 — Not Supported 0 1 0 — Not Supported 1 0 1 — Not Supported

Bus Arbitration:

Symbol	Pin #	I/O	Description
$\overline{AB\_BR}$	28	O	**ABus Bus Request:** This signal is used by the MACSI device to request use of the ABus.
$\overline{AB\_BG}$	27	I	**ABus Grant:** This signal is asserted by external bus arbitration logic to grant use of the ABus to the MACSI device. If $\overline{AB\_BG}$ is asserted at the start of a transaction (Tbr), the MACSI device will run a transaction. Note that in normal ABus mode (MR1.EAM = 0), the MACSI device may take up to two cycles to respond to $\overline{AB\_BG}$. Therefore, $\overline{AB\_BG}$ should not be removed until the MACSI device has indicated that it has sampled $\overline{AB\_BG}$ and taken the bus, (this can be determined with $\overline{AB\_AS}$ for example).
$\overline{AB\_CLK}$	38	I	**ABus Clock:** All ABus operations are synchronized to the rising edge of AB_CLK.

8.0 Signal Descriptions (Continued)

8.5 ELECTRICAL INTERFACE

Symbol	Pin #	I/O	Description
LBC5, 3	125, 126	I	**Local Byte Clock:** 12.5 MHz clocks with a 50/50 duty-cycle, generated by the PLAYER+ device.
LBC1	127	I	**Local Byte Clock:** 12.5 MHz clock with a 50/50 duty-cycle, generated by the PLAYER+. Connects to two pins on the MACSI device.
LSC	124	I	**Local Symbol Clock:** 25 MHz clock with a 40/60 duty-cycle, generated by the PLAYER+ device.
$\overline{RST}$	128	I	**Reset:** Active Low input which resets the Internal State Machines and most Registers. This signal must be asserted for at least five clock cycles. When asserted, all bidirectional signals are at TRI-STATE.
TCK	95	I	TCK: JTAG Scan Clock
TMS	94	I	TMS: JTAG Mode Select
TDI	93	I	TDI: JTAG Data In
TDO	92	O	TDO: JTAG Data Out
$\overline{TRST}$	91	I	TRST: JTAG Reset. Active low signal.
V_{CC}[11]	3, 17, 32, 43, 54, 66, 77, 97, 113, 135, 146		**Positive Power Supply:** 5V, 10% relative to GND.
GND[11]	4, 18, 33, 44, 55, 67, 78, 96, 112, 134, 145		**Ground:** Power Supply Return.
RSRVD0	88, 98–101	I	**Reserved 0:** Must be connected to ground.
N/C	26, 89		**No Connect:** Must be left unconnected.

9.0 Electrical Characteristics

9.1 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC}	Supply Voltage		−0.5		7.0	V
DC_{IN}	Input Voltage		−0.5		V_{CC} + 0.5	V
DC_{OUT}	Output Voltage		−0.5		V_{CC} + 0.5	V
T_{STG}	Storage Temperature		−65		150	°C
T_L	Lead Temperature	Soldering, 10 Sec. (IR or Vapor) (Phase Reflow)			230	°C
	ESD Protection		2000			V

9.2 RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC}	Supply Voltage		4.5		5.5	V
T_A	Operating Temperature		0		70	°C
PD	Power Dissipation			800		mW

9.3 DC ELECTRICAL CHARACTERISTICS

The DC characteristics are over the operating range, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	Output High Voltage	I_{OH} = −8 mA	2.4			V
V_{OL1}	Output Low Voltage	I_{OL} = 8 mA			0.4	V
V_{OL2}	Output Low Voltage for $\overline{INT0}$, $\overline{INT1}$, and $\overline{ACK}$ (open drain)	I_{OL} = 8 mA			0.4	V
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IL}	Input Low Current	V_{IN} = GND			−10	μA
I_{IH}	Input High Current	V_{IN} = V_{CC}			+10	μA
I_{OZ1}	TRI-STATE Leakage				±10	μA
I_{OZ2}	TRI-STATE Leakage for $\overline{INT0}$, $\overline{INT1}$, and $\overline{ACK}$ (open drain)				±10	μA
I_{CC}	Dynamic Supply Current	C_L = 50 pf, LBC = 12.5 MHz, AB__CLK = 25 MHz		145		mA

9.0 Electrical Characteristics (Continued)

9.4 AC ELECTRICAL CHARACTERISTICS

The AC Electrical characteristics are over the operating range, unless otherwise specified.

AC Characteristics for the Control Bus Interface

Symbol	Parameter Descriptions	Min	Max	Units
T1	$\overline{CE}$ Setup to LBC	15		ns
T2	LBC Period	80		ns
T3	LBC1 to $\overline{ACK}$ Low		45	ns
T4	$\overline{CE}$ Low to $\overline{ACK}$ Low	290	540	ns
T5	LBC1 Low to CBD(7-0) and CBP Valid		60	ns
T6	LBC1 to CBD(7-0) and CBP Active	5		ns
T7	$\overline{CE}$ Low to CBD(7-0) and CBP Active	225	475	ns
T8	$\overline{CE}$ Low to CBD(7-0) and CBP Valid	265	515	ns
T9	LBC Pulse Width High	35	45	ns
T10	LBC Pulse Width Low	35	45	ns
T11	$\overline{CE}$ High to $\overline{ACK}$ High		45	ns
T12	R/$\overline{W}$, CBA(7-0), CBD(7-0) and CBP Set up to $\overline{CE}$ Low	5		ns
T13	$\overline{CE}$ High to R/W, CBA(7-0), CBD(7-0) and CBP Hold Time	0		ns
T14	R/$\overline{W}$, CBA(7-0), CBD(7-0) and CBP to LBC1 Setup Time	20		ns
T15	$\overline{ACK}$ Low to $\overline{CE}$ High Lead Time	0		ns
T16	$\overline{CE}$ Minimum Pulse Width High	20		ns
T17	$\overline{CE}$ High to CBD(7-0) and CBP TRI-STATE		55	ns
T18	$\overline{ACK}$ High to $\overline{CE}$ Low	0		ns
T19	CBD(7-0) Valid to $\overline{ACK}$ Low Setup	20		ns
T20	LBC1 to $\overline{INT0}$, $\overline{INT1}$ Low		55	ns

Asynchronous Definitions

T4 (min)	T1 + (3 * T2) + T3
T4 (max)	T1 + (6 * T2) + T3
T7 (min)	T1 + (2 * T2) + T6
T7 (max)	T1 + (5 * T2) + T6
T8 (min)	T1 + (2 * T2) + T9 + T5
T8 (max)	T1 + (5 * T2) + T9 + T5

Note: Min/Max numbers are based on T2 = 80 ns and T9 = T10 = 40 ns.

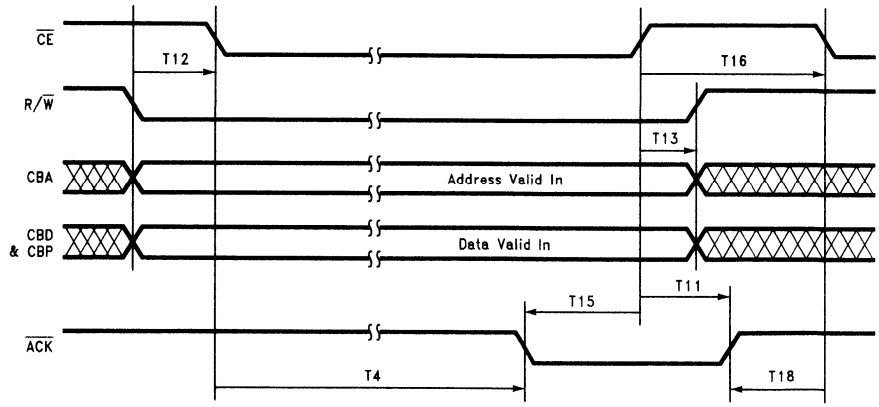


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FIGURE 9-1. Asynchronous Control Bus Write Cycle Timing

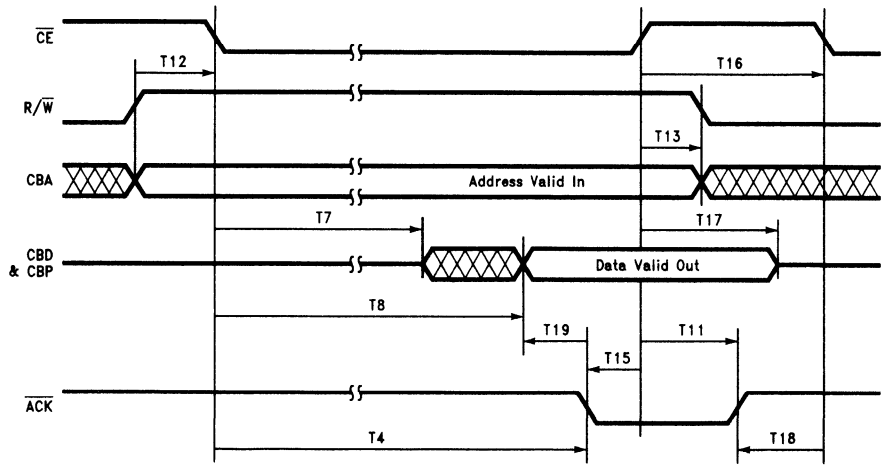

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FIGURE 9-2. Asynchronous Control Bus Read Cycle Timing

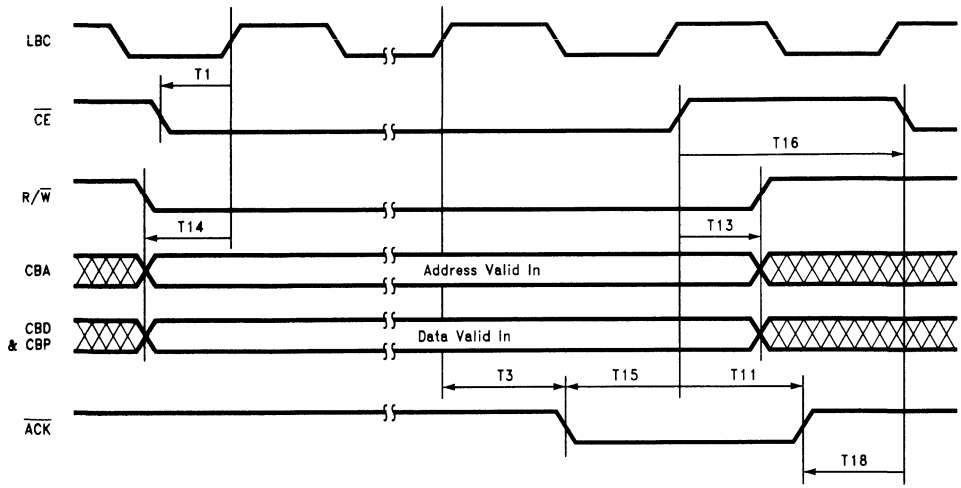

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FIGURE 9-3. Control Bus Synchronous Write Cycle Timing

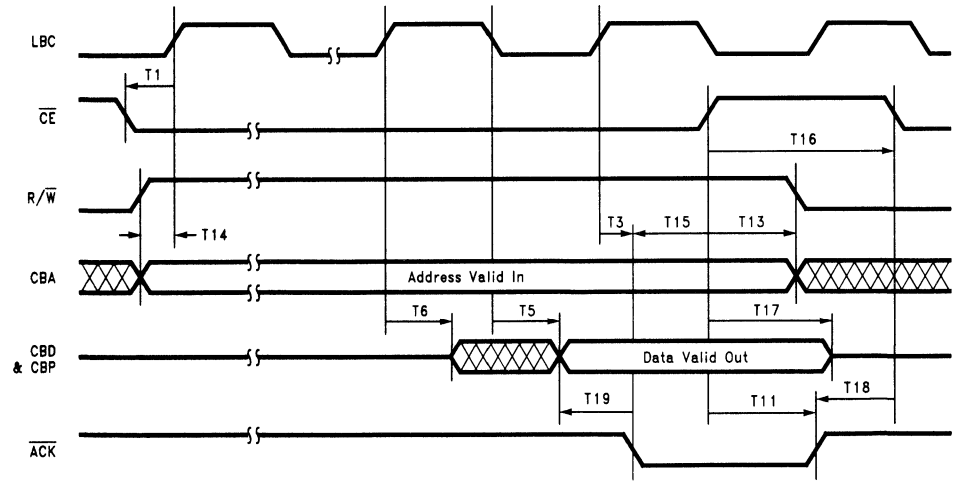

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FIGURE 9-4. Control Bus Synchronous Read Cycle Timing

9.0 Electrical Characteristics (Continued)

AC Characteristics for the Clock Interface Signals

Symbol	Parameter	Min	Typ	Max	Units
T21	LBC1 to LBC3 Lead time		16		ns
T22	LBC1 to LBC5 lead time		32		ns
T23	LBC1, LBC3, and LBC5 period		80		ns
T24	LBC1, LBC3, and LBC5 pulse width high		40		ns
T25	LBC1, LBC3, and LBC5 pulse width low		40		ns

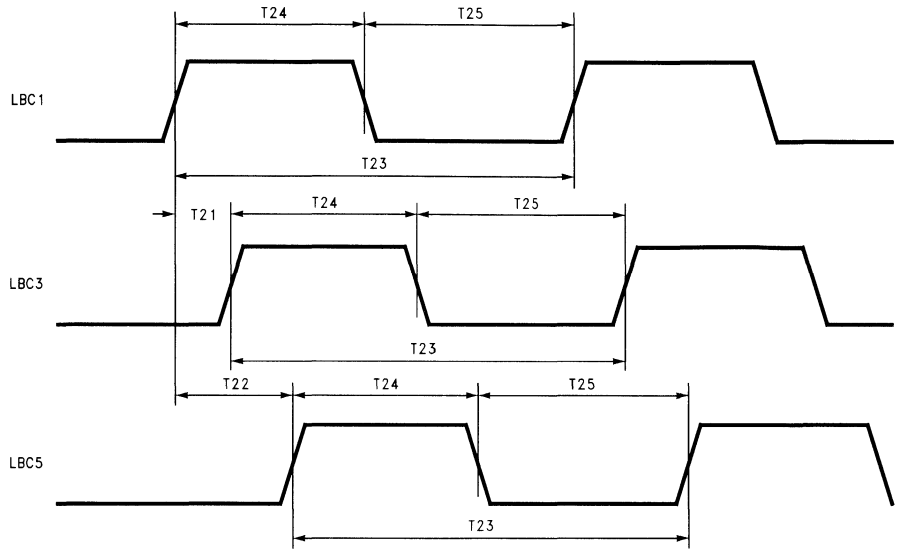

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FIGURE 9-5. Clock Interface Timing Diagram

9.0 Electrical Characteristics (Continued)

AC Characteristics for Port A Interface and Port B Interface

Symbol	Parameter	Min	Typ	Max	Units
T26	PHY Datal Inputs Setup to LBC1		15		ns
T27	PHY Data Inputs Hold from LBC1		0		ns
T28	PHY Data Outputs Sustain from LBC1		15		ns
T29	PHY Data Outputs LBC1 to Data Valid		30		ns
T32	ABus Outputs AB__CLK to TRI-STATE		15		ns
T33	AB__AD(31:0), AB__BP Output AB__CLK to Data Valid		12		ns
T34	AB__AD(31:0), AB__BP Output Sustain from AB__CLK		10		ns
T35	AB__AD(31:0), AB__BP Input Setup to AB__CLK		7		ns
T36	AB__AD(31:0), AB__BP Input Hold from AB__CLK		0		ns
T37	$\overline{\text{AB}}$__$\overline{\text{ACK}}$, $\overline{\text{AB}}$__$\overline{\text{BG}}$ Setup to AB__CLK		10		ns
T38	$\overline{\text{AB}}$__$\overline{\text{ACK}}$, $\overline{\text{AB}}$__$\overline{\text{BG}}$ Hold from AB__CLK		0		ns
T39	AB__ERR Setup to AB__CLK		10		ns
T40	AB__ERR Hold from AB__CLK		0		ns
T41	$\overline{\text{AB}}$__$\overline{\text{AS}}$, AB__SIZ(2:0), AB__$\overline{\text{RW}}$, $\overline{\text{AB}}$__$\overline{\text{DEN}}$ $\overline{\text{AB}}$__$\overline{\text{BR}}$, AB__A, Data Valid from AB__CLK		12		ns
T42	$\overline{\text{AB}}$__$\overline{\text{AS}}$, AB__SIZ(2:0), AB__$\overline{\text{RW}}$, $\overline{\text{AB}}$__$\overline{\text{DEN}}$ $\overline{\text{AB}}$__$\overline{\text{BR}}$, AB__A, Data sustain from AB__CLK		10		ns
F1	AB__CLK Operating Frequency AB__CLK Maximum Frequency	12.5 25	 33*	25	MHz MHz

*For guaranteed AB__CLK operation above 25 MHz, contact National Semiconductor.

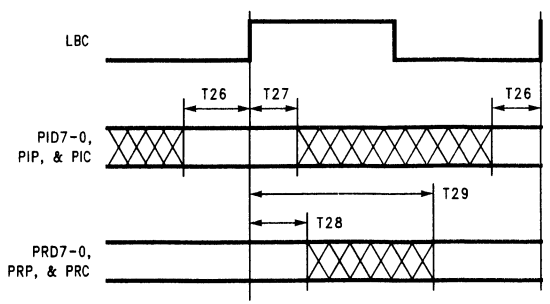

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FIGURE 9-6. PHY Interface Timing

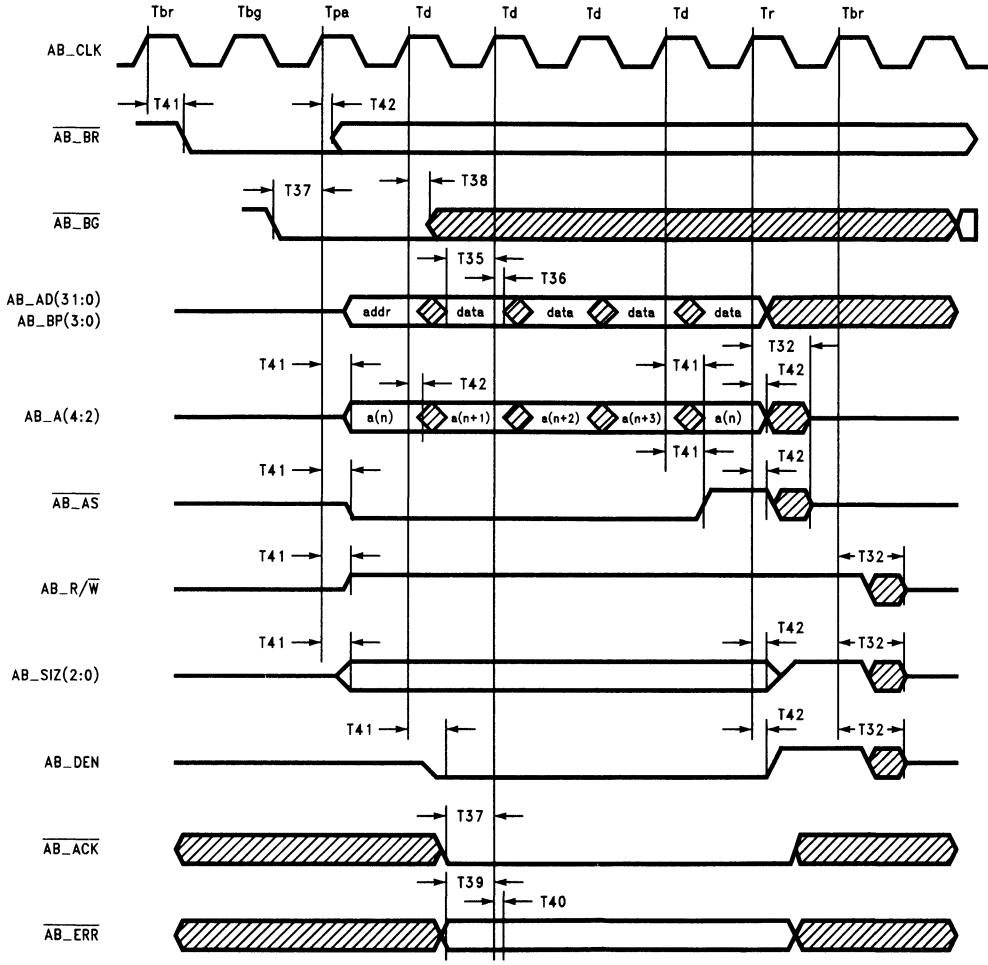

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FIGURE 9-7a. ABus Read Cycle Timing Diagram

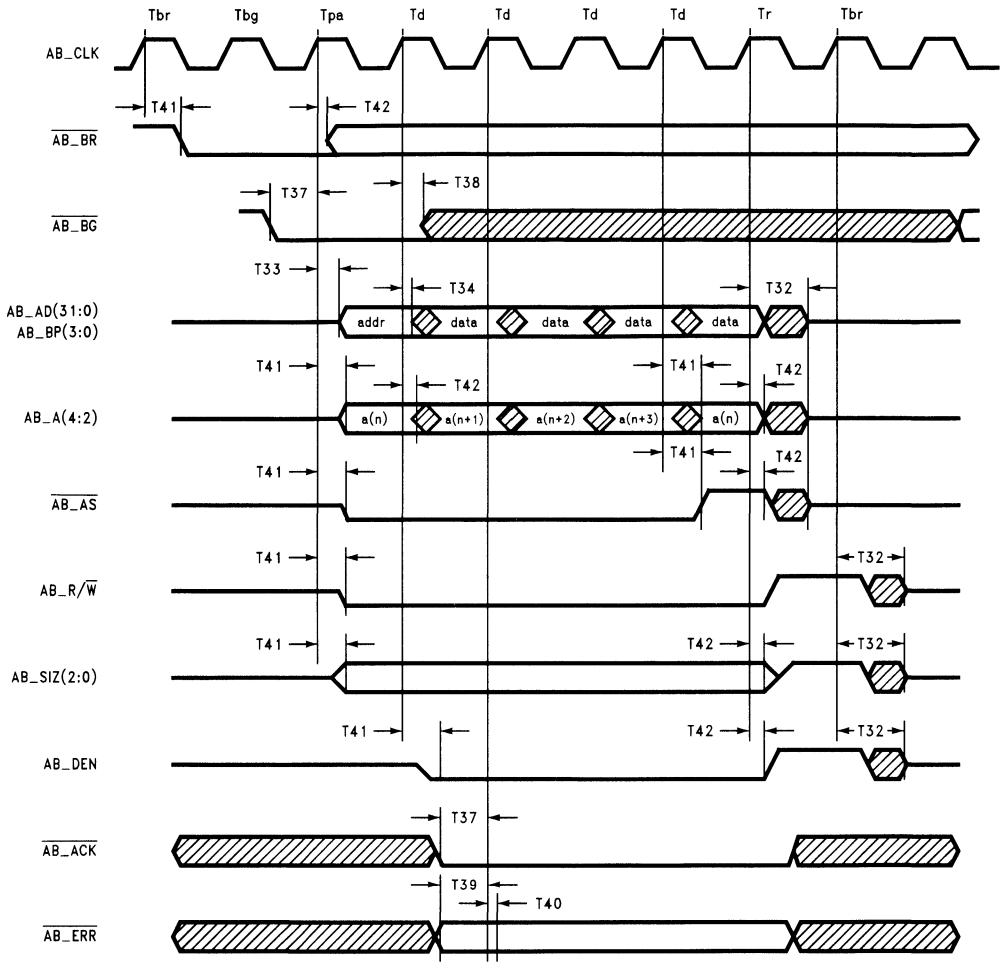

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Figure 9-7b. ABus Write Cycle Timing Diagram

9.0 Electrical Characteristics (Continued)

AC Signal Testing

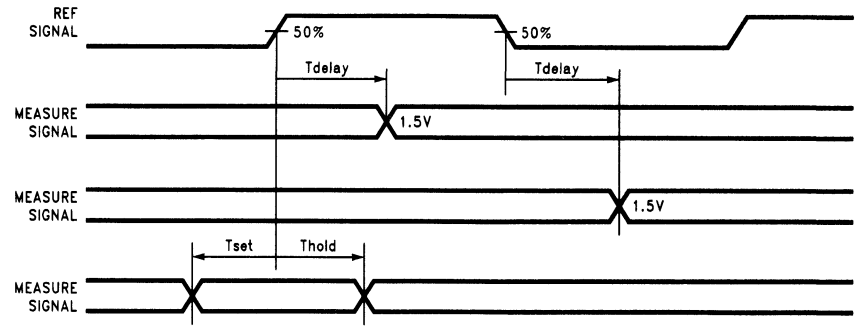

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FIGURE 9-8. AC Signal Testing

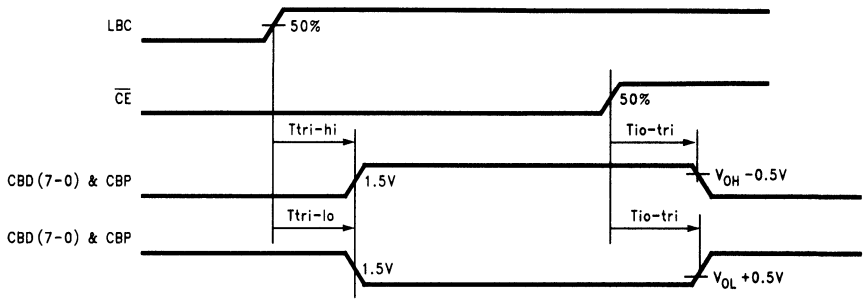

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FIGURE 9-9. TRI-STATE Timing

Test Conditions for AC Testing

V_{IH}	3.0V
V_{IL}	0.0V
V_{OH}	1.5V
V_{OL}	1.5V
C_L	50 pF

9.0 Electrical Characteristics (Continued)

Test Equivalent Loads

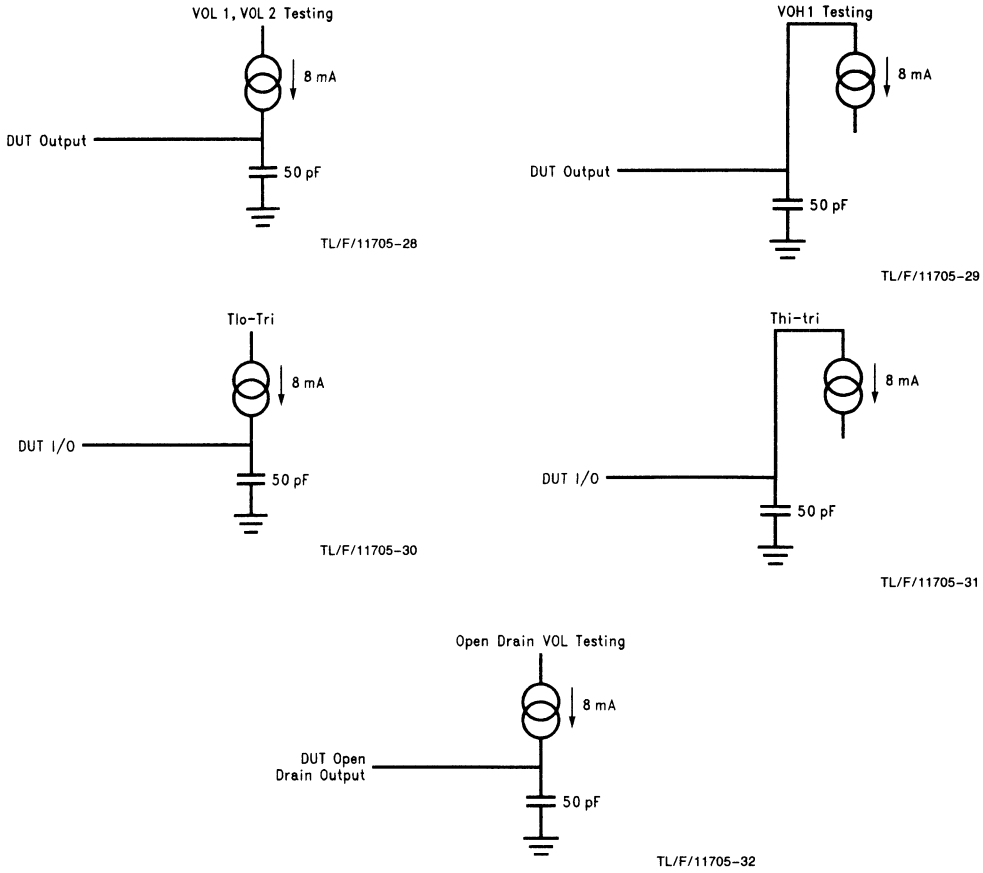

FIGURE 9-10. Test Equivalent Loads

10.0 Pin Table and Pin Diagram

Pin	Description	I/O
1	AB_A7	O
2	AB_A8	O
3	V_{CC}	
4	GND	
5	AB_A9	O
6	AB_A10	O
7	AB_A11	O
8	AB_A12	O
9	AB_A13	O
10	AB_A14	O
11	AB_A15	O
12	AB_A16	O
13	AB_A17	O
14	AB_A18	O
15	AB_A19	O
16	AB_A20	O
17	V_{CC}	
18	GND	
19	AB_A21	O
20	AB_A22	O
21	AB_A23	O
22	AB_A24	O
23	AB_A25	O
24	AB_A26	O
25	AB_A27	O
26	N/C	
27	$\overline{AB\_BG}$	I
28	$\overline{AB\_BR}$	O
29	AB_SIZ0	O
30	AB_SIZ1	O
31	AB_SIZ2	O
32	V_{CC}	
33	GND	
34	$\overline{AB\_DEN}$	I/O
35	AB_R/$\overline{W}$	O
36	$\overline{AB\_ERR}$	I
37	$\overline{AB\_ACK}$	I
38	AB_CLK	I
39	$\overline{AB\_AS}$	O
40	AB_AD31	I/O
41	AB_AD30	I/O
42	AB_AD29	I/O
43	V_{CC}	
44	GND	
45	AB_AD28	I/O
46	AB_AD27	I/O
47	AB_AD26	I/O
48	AB_AD25	I/O
49	AB_AD24	I/O
50	AD_BP3	I/O
51	AB_AD23	I/O
52	AB_AD22	I/O
53	AB_AD21	I/O
54	V_{CC}	
55	GND	
56	AB_AD20	I/O
57	AB_AD19	I/O
58	AB_AD18	I/O
59	AB_AD17	I/O
60	AB_AD16	I/O
61	AD_BP2	I/O
62	AB_AD15	I/O
63	AB_AD14	I/O
64	AB_AD13	I/O
65	AB_AD12	I/O
66	V_{CC}	
67	GND	
68	AB_AD11	I/O
69	AB_AD10	I/O
70	AB_AD9	I/O
71	AB_AD8	I/O
72	AB_BP1	I/O
73	AB_AD7	I/O
74	AB_AD6	I/O
75	AB_AD5	I/O
76	AB_AD4	I/O
77	V_{CC}	
78	GND	
79	AB_AD3	I/O
80	AB_AD2	I/O
81	AB_AD1	I/O
82	AB_AD0	I/O
83	AB_BP0	I/O
84	ECOPY	I
85	EA	I
86	ECIP	I
87	EM	I
88	RSRVD0	I
89	N/C	
90	LEARN	I
91	$\overline{TRST}$	I
92	TDO	O
93	TDI	I
94	TMS	I
95	TCK	I
96	GND	
97	V_{CC}	
98	RSRVD0	I
99	RSRVD0	I
100	RSRVD0	I
101	RSRVD0	I
102	PRD0	O
103	PID0	I
104	PRD1	O
105	PID1	I
106	PRD2	O
107	PID2	I
108	PRD3	O
109	PID3	I
110	PRD4	O
111	PID4	I
112	GND	
113	V_{CC}	
114	PRD5	O
115	PID5	I
116	PRD6	O
117	PID6	I
118	PRD7	O
119	PID7	I
120	PRC	O
121	PIC	I
122	PRP	O
123	PIP	I
124	LSC	I
125	LBC5	I
126	LBC3	I
127	LBC1	I
128	$\overline{RST}$	I
129	R/$\overline{W}$	I
130	$\overline{CE}$	I
131	$\overline{INT1}$	OD
132	$\overline{INT0}$	OD
133	$\overline{ACK}$	O
134	GND	
135	V_{CC}	
136	CBA0	I
137	CBA1	I
138	CBA2	I
139	CBA3	I
140	CBA4	I
141	CBA5	I
142	CBA6	I
143	CBA7	I
144	CBA8	I
145	GND	
146	V_{CC}	
147	CBD0	I/O
148	CBD1	I/O
149	CBD2	I/O
150	CBD3	I/O
151	CBD4	I/O
152	CBD5	I/O
153	CBD6	I/O
154	CBD7	I/O
155	CBP	I/O
156	AB_A2	O
157	AB_A3	O
158	AB_A4	O
159	AB_A5	O
160	AB_A6	O

10.0 Pin Table and Pin Diagram (Continued)

The pinout of the MACSI device is shown in the diagram below.

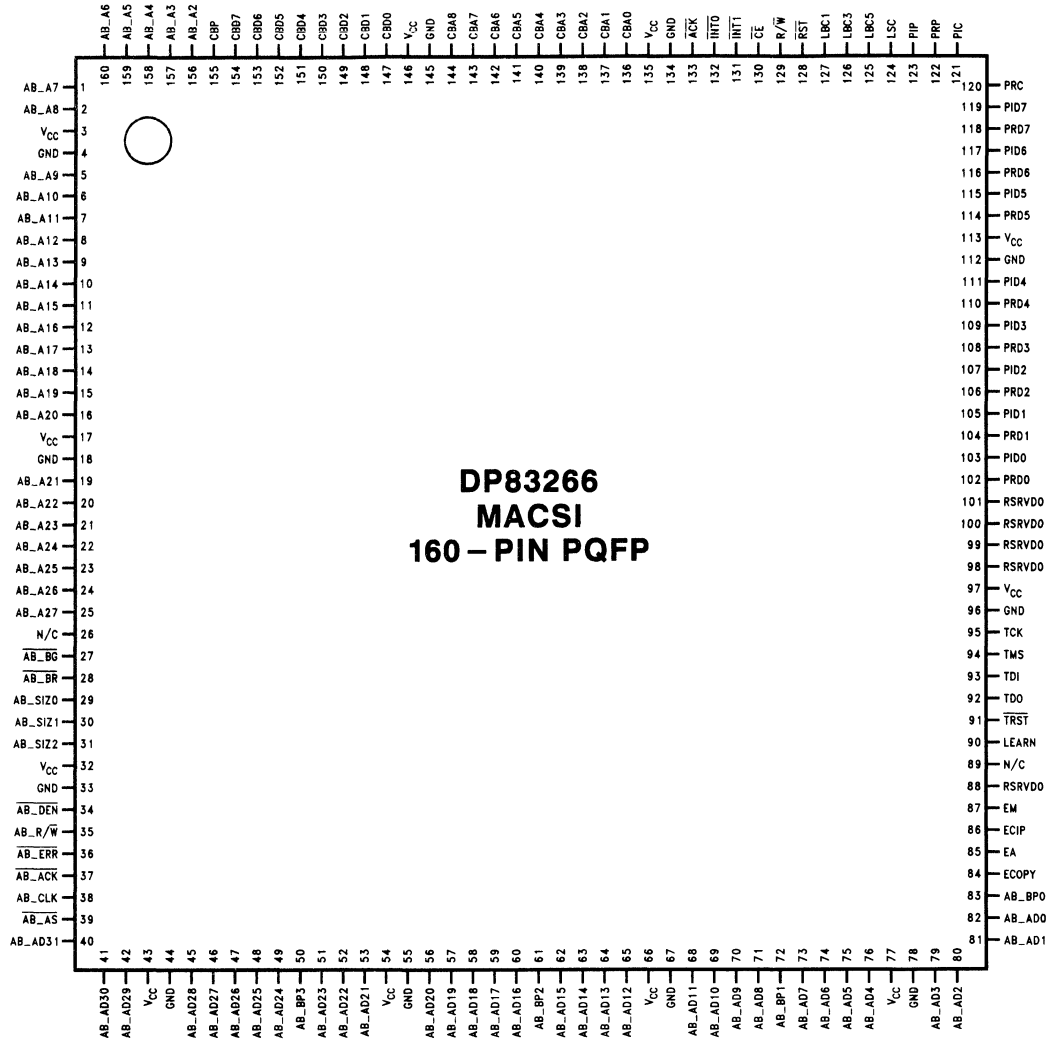

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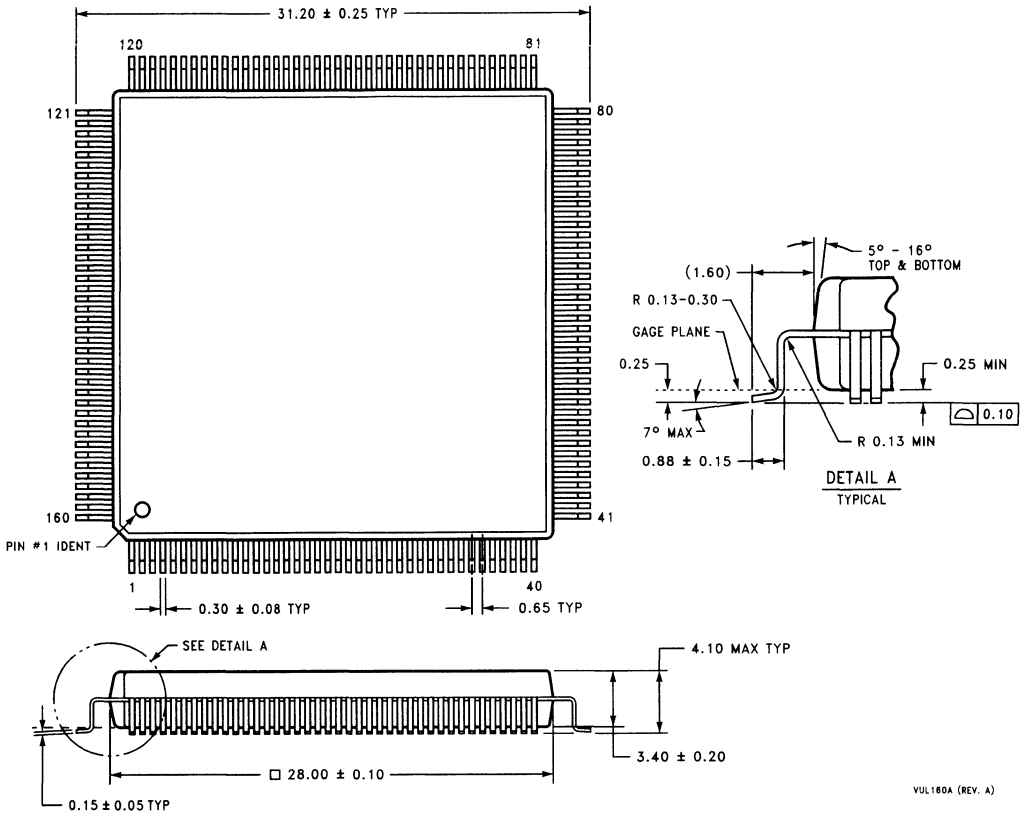
FIGURE 10-1. DP83266 Pinout

Physical Dimensions inches (millimeters)



Plastic Quad Flat Pack (VUL)
Order Number DP83266VF
NS Package Number VUL160A

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DP83256/DP83257 PLAYER+ Device (FDDI Physical Layer Controller)

National Semiconductor

PRELIMINARY
October 1992

DP83256/DP83257
PLAYER+™ Device (FDDI Physical Layer Controller)

General Description

The DP83256/DP83257 Enhanced Physical Layer Controller (PLAYER+ device) implements one complete Physical Layer (PHY) entity as defined by the Fiber Distributed Data Interface (FDDI) ANSI X3T9.5 standard.

The PLAYER+ device integrates state of the art digital clock recovery and improved clock generation functions to enhance performance, eliminate external components and remove critical layout requirements.

FDDI Station Management (SMT) is aided by Link Error Monitoring support, Noise Event Timer (TNE) support, Optional Auto Scrubbing support, an integrated configuration switch and built-in functionality designed to remove all stringent response time requirements such as PC_React and CF_React.

Features

- Single chip FDDI Physical Layer (PHY) solution
- Integrated Digital Clock Recovery Module provides enhanced tracking and greater lock acquisition range
- Integrated Clock Generation Module provides all necessary clock signals for an FDDI system from an external 12.5 MHz reference
- Alternate PMD Interface (DP83257) supports UTP twisted pair FDDI PMDs with no external clock recovery or clock generation functions required
- No External Filter Components
- Connection Management (CMT) Support (LEM, TNE, PC_React, CF_React, Auto Scrubbing)
- Full on-chip configuration switch
- Low Power CMOS-BIPOLAR design using a single 5V supply
- Full duplex operation with through parity
- Separate management interface (Control Bus)
- Selectable Parity on PHY-MAC Interface and Control Bus Interface
- Two levels of on-chip loopback
- 4B/5B encoder/decoder
- Framing logic
- Elasticity Buffer, Repeat Filter, and Smoother
- Line state detector/generator
- Supports single attach stations, dual attach stations and concentrators with no external logic
- DP83256 for SAS/DAS single path stations
- DP83257 for SAS/DAS single/dual path stations

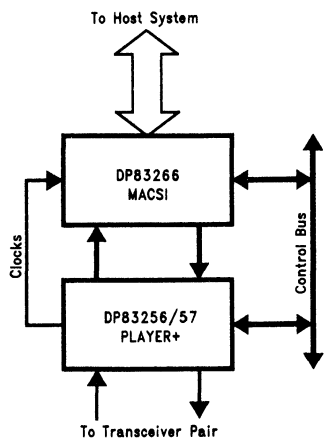

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FIGURE 1-1. FDDI Chip Set Overview

Table of Contents

1.0 FDDI Chip Set Overview

National Semiconductor's next generation FDDI chip set consists of two components as shown in *Figure 1-1*. The PLAYER+ device integrates the features of the DP83231 CRD™ Clock Recovery Device, DP83241 CDD™ Clock Distribution Device, and DP83251/55 PLAYER™ Physical Layer Controller. In addition, the PLAYER+ device contains enhanced SMT support.

For more information on the other devices of the chip set, consult the appropriate datasheets and application notes.

DP83256/57 PLAYER+ Device Physical Layer Controller

The PLAYER+ device implements the Physical Layer (PHY) protocol as defined by the ANSI FDDI PHY X3T9.5 standard.

Features

- Single chip FDDI Physical Layer (PHY) solution
- Integrated Digital Clock Recovery Module provides enhanced tracking and greater lock acquisition range
- Integrated Clock Generation Module provides all necessary clock signals for an FDDI system from an external 12.5 MHz reference
- Alternate PMD Interface (DP83257) supports UTP twisted pair FDDI PMDs with no external clock recovery or clock generation functions required
- No External Filter Components
- Connection Management (CMT) Support (LEM, TNE, PC_React, CF_React, Auto Scrubbing)
- Full on-chip configuration switch
- Low Power CMOS-BIPOLAR design using a single 5V supply
- Full duplex operation with through parity
- Separate management interface (Control Bus)
- Selectable Parity on PHY-MAC Interface and Control Bus Interface
- Two levels of on-chip loopback
- 4B/5B encoder/decoder
- Framing logic
- Elasticity Buffer, Repeat Filter, and Smoother
- Line state detector/generator
- Supports single attach stations, dual attach stations and concentrators with no external logic
- DP83256 for SAS/DAS single path stations
- P83257 for SAS/DAS single/dual path stations

In addition, the DP83257 contains the additional PHY_Data.request and PHY_Data.indicate ports required for concentrators and dual attach, dual path stations.

DP83266 MACSI™ Device Media Access Controller and System Interface

The DP83266 Media Access Controller and System Interface (MACSI) implements the ANSI X3T9.5 Standard Media Access Control (MAC) protocol for operation in an FDDI token ring and provides a comprehensive System Interface.

The MACSI device transmits, receives, repeats, and strips tokens and frames. It produces and consumes optimized data structures for efficient data transfer. Full duplex architecture with through parity allows diagnostic transmission and self testing for error isolation in point-to-point connections.

The MACSI device includes the functionality of both the DP83261 BMAC device and the DP83265 BSI-2 device with additional enhancements for higher performance and reliability.

Features

- Over 9 Kbytes of on-chip FIFO
- 5 DMA Channels (2 Output and 3 Input)
- 12.5 MHz to 33 MHz operation
- Full duplex operation with through parity
- Real-time VOID frame stripping indicator for bridges
- On-chip Address bit swapping capability
- 32-bit wide Address/Data path with byte parity
- Programmable transfer burst sizes of 4 or 8 32-bit words
- Receive frame filtering services
- Frame-per-Page mode controllable on each DMA channel
- Demultiplexed Addresses supported on ABus
- New multicast address matching
- ANSI X3T9.5 MAC standard defined ring service options
- Supports all FDDI Ring Scheduling Classes (Synchronous, Asynchronous, etc.)
- Supports Individual, Group, Short, Long, and External Addressing.
- Generates Beacon, Claim, and Void frames
- Extensive ring and station statistics gathering
- Extension for MAC level bridging
- Enhanced SBus compatibility
- Interfaces to DRAMs or directly to system bus
- Supports frame Header/Info splitting
- Programmable Big or Little Endian alignment

2.0 Architecture Description

2.1 BLOCK OVERVIEW

The PLAYER+ device is comprised of six blocks: Clock Recovery, Receiver, Configuration Switch, Transmitter, Station Management (SMT) Support, and Clock Generation Module as shown in *Figure 2-1*.

Clock Recovery

The Clock Recovery Module accepts a 125 Mbps NRZI data stream from the external PMD receiver. It then provides the extracted and synchronized data and clock to the Receiver block.

The Clock Recovery Module performs the following operations:

- Locks to and tracks the incoming NRZI data stream
- Extracts data stream and synchronized 125 MHz clock

Receiver

During normal operation, the Receiver Block accepts serial data as inputs at the rate of 125 Mbps from the Clock Recovery Module. During the Internal Loopback mode of operation, the Receiver Block accepts data directly from the Transmitter Block.

The Receiver Block performs the following operations:

- Optionally converts the incoming data stream from NRZI to NRZ.
- Decodes the data from 5B to 4B coding.
- Converts the serial bit stream into 10-bit bytes composed of 8 bits data, 1 bit parity, and 1 bit control information.
- Compensates for the differences between the upstream station clock and the local clocks.
- Decodes Line States.
- Detects link errors.
- Presents data symbol pairs (bytes) to the Configuration Switch Block.

Configuration Switch

An FDDI station may be in one of three configurations: Isolate, Wrap or Thru. The Configuration Switch supports these configurations by switching the transmitted and received data paths between PLAYER+ devices and one or more MACSI devices.

The configuration switch is integrated into the PLAYER+ device, therefore no external logic is required for this function.

Setting the Configuration switch can be done explicitly via the Control Bus Interface or it can be set automatically with the CF_React SMT Support feature.

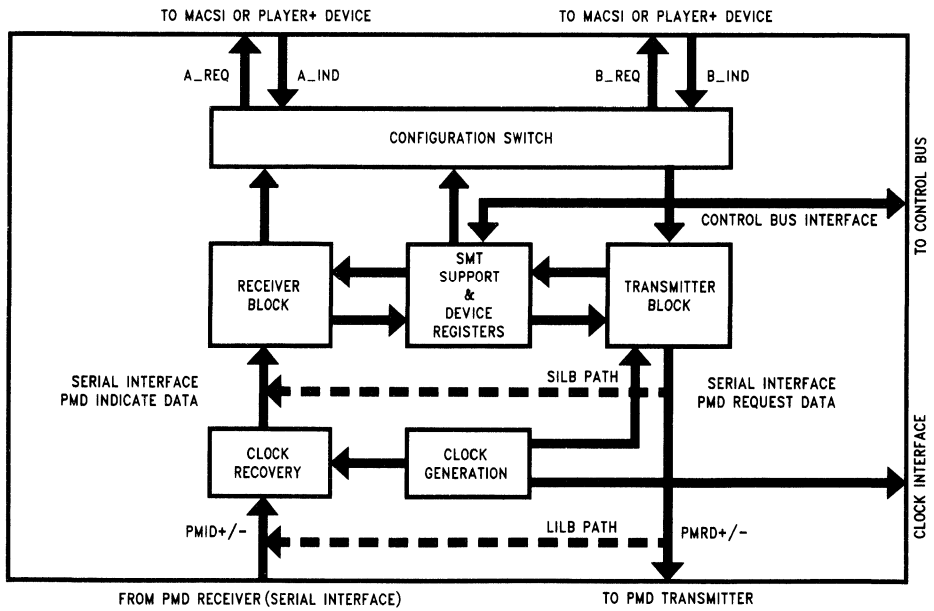

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FIGURE 2-1. PLAYER+ Device Block Diagram

2.0 Architecture Description (Continued)

Transmitter

The Transmitter Block accepts 10-bit bytes composed of 8 bits data, 1 bit parity, and 1 bit control information from the Configuration Switch.

The Transmitter Block performs the following operations:

- Encodes the data from 4B to 5B coding.
- Filters out code violations from the data stream.
- Generates Idle, Master, Halt, Quiet, or other user defined symbol pairs upon request.
- Converts the data stream from NRZ to NRZI format for transmission.
- Provides smoothing function when necessary.

During normal operation, the Transmitter Block presents serial data to the PMD transmitter. While in Internal Loopback mode, the Transmitter Block presents serial data to the Receiver Block. While in the External Loopback mode, the Transmitter Block presents serial data to the Clock Recovery Module.

Clock Generation Module

The Clock Generation Module is an integrated phase locked loop that generates all of the required clock signals for the PLAYER+ device and an FDDI system from a single 12.5 MHz reference.

The Clock Generation Module features:

- High precision clock timing generated from a single 12.5 MHz reference.
- Multiple precision phased (8 ns/16 ns) 12.5 MHz Local Byte Clocks to eliminate timing skew in large multi-board concentrator configurations.
- LBC timing which is insensitive to loading variations over a wide range (20 pF to 70 pF) of LBC loads.
- A selectable dual frequency system clock.
- Low clock edge jitter, due to high VCO stability.

Station Management (SMT) Support

The Station Management Support Block provides a number of useful features to simplify the implementation of the Connection Management (CMT) portion of SMT.

These features eliminate the time critical CMT response time constraints imposed by PC_React and CF_React times.

Integrated counters and timers eliminate the need for additional external devices.

The following are the CMT features supported:

- PC_React
- CF_React
- Auto Scrubbing (TCF Timer)
- Timer, Idle Detection (TID Timer)
- Noise Event Counter (TNE Timer)
- Link Error Monitor (LEM Counter)

2.2 INTERFACES

The PLAYER+ device connects to other devices via five functional interfaces: PMD Interface, PHY Port Interface, Control Bus Interface, Clock Interface, and the Miscellaneous Interface.

PMD Interface

The PMD Interface connects the PLAYER+ device to a standard FDDI Physical Media Connection such as a fiber optic transceiver or a copper twisted pair transceiver. It is a 125 MHz full duplex serial connection.

The DP83257 PLAYER+ device contains two PMD interfaces. The Primary PMD Interface should be used for all PMD implementations that do not require an external scrambler/descrambler function, clock recovery function, or clock generation function, such as a Fiber Optic or Shielded Twisted Pair (SDDI) PMD. The second, Alternate PMD Interface can be used to support Unshielded Twisted Pair (UTP) PMDs that require external scrambling, and allows implementation with no external clock recovery or clock generation functions required.

PHY Port Interface

The PHY Port Interface connects the PLAYER+ device to one or more MAC devices and/or PLAYER+ devices. Each PHY Port Interface consists of two byte-wide interfaces, one for PHY Request data input to the PLAYER+ device and one for the PHY Indicate data output of the PLAYER+ device. Each byte-wide interface consists of a parity bit (odd parity), a control bit, and two 4-bit symbols.

The DP83257 PLAYER+ device has two PHY Port Interfaces while the DP83256 has one PHY Port Interface.

Control Bus Interface

The Control Bus Interface connects the PLAYER+ device to a wide variety of microprocessors and microcontrollers. The Control Bus is an asynchronous interface which provides access to 64 8-bit registers which monitor and control the behavior of the PLAYER+ device.

The Control Bus Interface allows a user to:

- Configure SMT features.
- Program the Configuration Switch.
- Enable/disable functions within the Transmitter and Receiver Blocks (i.e., NRZ/NRZI Encoder, Smoother, PHY Request Data Parity, Line State Generation, Symbol pair Injection, NRZ/NRZI Decoder, Cascade Mode, etc.).

The Control Bus Interface also can be used to perform the following functions:

- Monitor Line States received.
- Monitor link errors detected by the Receiver Block.
- Monitor other error conditions.

Clock Interface

The Clock Interface is used to configure the Clock Generation Module and to provide the required clock signals for an FDDI system.

The following clock signals are generated:

- 5 phase offset 12.5 MHz Local Byte Clocks
- 25 MHz Local Symbol Clock
- 15.625 or 31.25 MHz System Clock

Miscellaneous Interface

The Miscellaneous Interface consists of:

- A reset signal.
- User definable sense signals.
- User definable enable signals.
- Synchronization for cascading PLAYER+ devices (a high-performance non-FDDI mode).
- Device Power and Ground pins.

3.0 Functional Description

The PLAYER+ device is comprised of six blocks: Clock Recovery, Receiver, Transmitter, Configuration Switch, Clock Generation, and Station Management Support.

3.1 CLOCK RECOVERY MODULE

The Clock Recovery Module accepts a 125 Mbps NRZI data stream from the external PMD receiver. It then provides the extracted and synchronized data and clock to the Receiver block.

The Clock Recovery Module performs the following operations:

- Locks onto and tracks the incoming NRZI data stream
- Extracts the data stream and the synchronized 125 MHz clock

The Clock Recovery Module is implemented using an advanced digital architecture that replaces sensitive analog blocks with digital circuitry. This allows the PLAYER+ device to be manufactured to tighter tolerances since it is less sensitive to processing variations that can adversely affect analog circuits.

The Clock Recovery Module is comprised of 5 main functional blocks:

Digital Phase Detector

Digital Phase Error Processor

Digital Loop Filter

Digital Phase to Frequency Converter

Frequency Controlled Oscillator

See *Figure 3-1*, Clock Recovery Module Block Diagram.

DIGITAL PHASE DETECTOR

The Digital Phase Detector has two main functions: phase error detection and data recovery.

Phase error detection is accomplished by a digital circuit that compares the input data (PMID) to an internal phase-locked 125 MHz reference clock and generates a pair of error signals. The first signal is a pulse whose width is equal to the phase error between the input data and a reference clock and the second signal is a 4 ns reference pulse. These signals are fed into the Digital Phase Error Processor block.

The data recovery function converts the incoming encoded data stream (PMID) into synchronized data and clock signals. When the circuit is in lock the rising edge of the recovered clock is exactly centered in the recovered data bit cell.

The digital phase detector uses a common path for phase error detection and data recovery so as to minimize clock Static Alignment Error (SAE). Phase error averaging is also included so that phase errors generated by positive and negative PMID edges equally affect the clock recovery circuit. This greatly improves the immunity to Duty Cycle Distortion (DCD) in the data recovery circuit.

DIGITAL PHASE ERROR PROCESSOR

The Digital Phase Error Processor is responsible for sampling the Phase Detector's phase error outputs and producing two digital outputs that indicate to the digital loop filter how to adjust for a difference between the data phase and reference phases.

The Phase Error Processor is designed to eliminate the effects of different clock edge densities between data symbols and the various line state symbols on the PLL's loop gain.

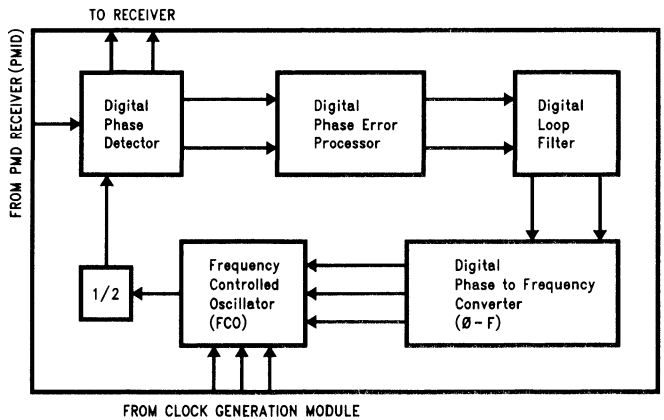

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FIGURE 3-1. Clock Recovery Module Block Diagram

3.0 Functional Description (Continued)

Since the loop gain is held constant regardless of the incoming signal edge density, PLL characteristics such as jitter, acquisition rate, locking range etc., are deterministic and show minimal spread under various operating environments.

The phase error processor also automatically puts the loop in open-loop-mode when the incoming data stream contains abnormal low edge rates. When the PLL is in open-loop-mode, no update is made to the PLL's filter variables in the filter block. The PLL can then use the pretrained frequency and phase contents to perform data recovery. Since the loop is implemented digitally, these values (the frequency and phase variables) are retained. The resolution of the frequency variable is about 1.3 ppm of the incoming frequency. The resolution of the phase variable is about 40 ps.

DIGITAL LOOP FILTER

The digital loop filter emulates a 1-pole, 1-zero filter and uses an automatic acquisition speed control circuit to dynamically adjust loop parameters.

The digital loop filter takes the phase error indicator signals Data Valid and Up/Down from the Phase Error processor and accumulates errors over a few cycles before passing on the Data Valid and Up/Down signals to the Phase Error to Frequency converter.

The filter has 4 sets of bandwidth and damping parameters which are switched dynamically by an acquisition control circuit. The input Signal Detect (SD) starts the sequence and, thereafter, no user programming is required to finish the sequence.

At the completion of the locking sequence, the loop has the narrowest bandwidth such that the loop produces minimal recovered clock jitter. The PLL can track an incoming frequency offset of approximately ±200 ppm. After the acquisition sequence, the equivalent natural frequency of the loop is reduced to about 7 kHz (±56 ppm) of frequency offset.

The automatic tracking mechanism allows the loop to quickly lock onto the initial data stream for data recovery (typically less than 10 μs) and yet produce very little recovered clock jitter.

PHASE ERROR TO FREQUENCY CONVERTER (∅-F)

The Phase Error to Frequency Converter takes the Data Valid and Up/Down signals modified by the Digital Loop Filter and converts them to triangle waves. The frequency of the triangle waves is then used to control the Frequency Controlled Oscillator's (FCO) 250 MHz oscillations.

Each valid Up or Down signal causes a partial 7-bit counter (using only 96 counts) to increment or decrement at the ∅-F converter's clock rate of 15.625 MHz (250 MHz/16). When the Data Valid signal is not asserted, the counter holds count.

The counter value is used to produce 3 triangle waves that are offset in phase by 120 degrees. This is done with a special Pulse Density Modulator waveform synthesizer which takes the place of a traditional Digital-Analog converter. The frequency of the triangle waves tells the Frequency Controlled Oscillator how much to adjust oscillation. The phase relationships (leading or lagging) between the 3 signals indicates the direction of change.

The minimum frequency of the triangle waves is 0 and corresponds to the case when the PLL is in perfect lock with the incoming signal.

The maximum frequency that the ∅-F converter can produce determines the locking range of the PLL. In this case the maximum frequency of each triangle wave is 162.76 kHz, which is produced when the ∅-F converter gets a continuous count in one direction that is valid every ∅-F converter clock cycle of 15.625 MHz (250 MHz/16). The triangle waves have an amplitude resolution of 48 digital steps, so a full rising and falling period takes 96 counts which produces a maximum frequency of 162.76 kHz (1/(1/15.625 kHz * 96)).

The 96 digital counts of the triangle waves also lead to a very fine PLL phase resolution of 42 ps (4 ns/96 counts). This high phase resolution is achieved using very low frequency signals, in contrast to a standard PLL which must operate at significantly higher frequencies than the data being tracked to achieve such high phase resolution.

FREQUENCY CONTROLLED OSCILLATOR (FCO)

The frequency controlled oscillator produces a 250 MHz clock that, when divided by 2, is phase locked to the incoming data's clock.

The FCO uses three 250 MHz reference clock signals from the Clock Generation Module and three 0 Hz to 162.76 kHz error clock signals from the Phase Error to Frequency Converter as inputs. Each signal in a triplet is 120 degrees phase shifted from the next.

Each corresponding pair (one 250 MHz and one error signal) of signals is mixed together using an amplitude switching modulator, with the error signal modulating the reference. All of the outputs are then summed together to produce the final 250 MHz $+f_m$ phase locked clock signal, where f_m is the error frequency.

3.2 RECEIVER BLOCK

During normal operation, the Receiver Block accepts serial data input at the rate of 125 Mbps from the Clock Recovery Module. During the Internal Loopback mode of operation, the Receiver Block accepts input data from the Transmitter Block.

The Receiver Block performs the following operations:

- Optionally converts the incoming data stream from NRZI to NRZ.
- Decodes the data from 5B to 4B coding.
- Converts the serial bit stream into the National byte-wide code.
- Compensates for the differences between the upstream station clock and the local clock.
- Decodes Line States.
- Detects link errors.
- Presents data symbol pairs to the Configuration Switch Block.

The Receiver Block consists of the following functional blocks:

NRZI to NRZ Decoder

Shift Register

Framing Logic

Symbol Decoder

3.0 Functional Description (Continued)

Line State Detector

Elasticity Buffer

Link Error Detector

See *Figure 3-2.*

NRZI TO NRZ DECODER

The NRZI to NRZ Decoder converts Non-Return-To-Zero-Invert-On-Ones data to Non-Return-To-Zero format.

NRZ format data is the natural data format that the receiver block utilizes internally, so this function is required when the standard NRZI format data is fed into the device. The receiver block can bypass this conversion function in the case where an alternate data source outputs NRZ format data.

This function can be enabled and disabled through bit 7 (RNRZ) of the Mode Register (MR). When the bit is cleared, it converts the incoming bit stream from NRZI to NRZ. This is the normal configuration required. When the bit is set, the incoming NRZ bit stream is passed unchanged.

SHIFT REGISTER

The Shift Register converts the serial bit stream into symbol-wide data for the 5B/4B Decoder.

The Shift Register also provides byte-wide data for the Framing Logic.

FRAMING LOGIC

The Framing Logic performs the Framing function by detecting the beginning of a frame or the Halt-Halt or Halt-Quiet symbol pair.

The J-K symbol pair (11000 10001) indicates the beginning of a frame during normal operation. The Halt-Halt (00100 00100) and Halt-Quiet (00100 00000) symbol pairs are detected for Connection Management (CMT).

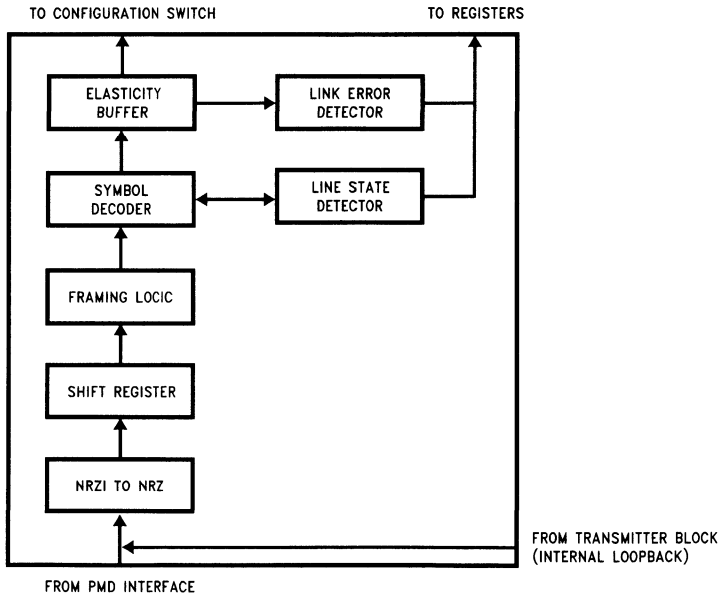

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FIGURE 3-2. Receiver Block Diagram

3.0 Functional Description (Continued)

Framing may be temporarily suspended (i.e. framing hold), in order to maintain data integrity.

Detecting JK

The JK symbol pair can be used to detect the beginning of a frame during Active Line State (ALS) and Idle Line State (ILS) conditions.

While the Line State Detector indicates Idle Line State the receiver "reframes" upon detecting a JK symbol pair and enters the Active Line State.

During Active Line State, acceptance of a JK symbol (reframing) is allowed for any on-boundary JK which is detected at least 1.5 byte times after the previous JK.

During Active Line State, once reframed on a JK, a subsequent off-boundary JK is ignored, even if it is detected beyond 1.5 byte times after the previous JK.

During Active Line State, an Idle or Ending Delimiter (T) symbol will allow reframing on any subsequent JK, if a JK is detected at least 1.5 byte times after the previous JK.

Detecting HALT-HALT AND HALT-QUIET

During Idle Line State, the detection of a Halt-Halt, or Halt-Quiet symbol pair will still allow the reframing of any subsequent on-boundary JK.

Once a JK is detected during Active Line State, off-boundary Halt-Halt, or Halt-Quiet symbol pairs are ignored until the Elasticity Buffer (EB) has an opportunity to recenter. They are treated as violations.

After recentering on a Halt-Halt, or Halt-Quiet symbol pair, all off boundary Halt-Halt or Halt-Quiet symbol pairs are ignored until the EB has a chance to recenter during a line state other than Active Line State (which may be as long as 2.8 byte times).

SYMBOL DECODER

The Symbol Decoder is a two level system. The first level is a 5-bit to 4-bit converter, and the second level is a 4-bit symbol pair to byte-wide code converter.

The first level latches the received 5-bit symbols and decodes them into 4-bit symbols. Symbols are decoded into two types: data and control. The 4-bit symbols are sent to the Line State Detector and the second level of the Symbol Decoder. See Table 3-1 for the 5B/4B Symbol Decoding list.

The second level translates two symbols from the 5B/4B converter and the line state information from the Line State Detector into the National byte-wide code.

LINE STATE DETECTOR

The ANSI X3T9.5 FDDI Physical Layer (PHY) standard specifies eight Line States that the Physical Layer can transmit. These Line States are used in the Connection Management process. They are also used to indicate data within a frame during normal operation.

The Line States are reported through the Current Receive State Register (CRSR), Receive Condition Register A (RCRA), and Receive Condition Register B (RCRB).

TABLE 3-1. 5B/4B Symbol Decoding

Symbol	Incoming 5B	Decoded 4B
0	11110	0000
1	01001	0001
2	10100	0010
3	10101	0011
4	01010	0100
5	01011	0101
6	01110	0110
7	01111	0111
8	10010	1000
9	10011	1001
A	10110	1010
B	10111	1011
C	11010	1100
D	11011	1101
E	11100	1110
F	11101	1111
I (Idle)	11111	1010
H (Halt)	00100	0001
JK (Starting Delimiter)	11000 and 10001	1101
T (Ending Delimiter)	01101	0101
R (Reset)	00111	0110
S (Set)	11001	0111
Q (Quiet)	00000	0010
V (Violation)	00001	0010
V	00010	0010
V	00011	0010
V	00101	0010
V	00110	0010
V	01000	0010
V	01100	0010
V	10000	0010

Note: V' denotes PHY Invalid or an Elasticity Buffer stuff byte
I' denotes Idle symbol in ILS or an Elasticity Buffer stuff byte

LINE STATES DESCRIPTION

Active Line State

The Line State Detector recognizes the incoming data to be in the Active Line State upon the reception of the Starting Delimiter (JK symbol pair).

The Line State Detector continues to indicate Active Line State while receiving data symbols, Ending Delimiter (T symbols), and Frame Status symbols (R and S) after the JK symbol pair.

Idle Line State

The Line State Detector recognizes the incoming data to be in the Idle Line State upon the reception of 2 Idle symbol pairs nominally (plus up to 9 bits of 1 in start up cases).

Idle Line State indicates the preamble of a frame or the lack of frame transmission during normal operation. Idle Line State is also used in the handshake sequence of the PHY Connection Management process.

3.0 Functional Description (Continued)

Super Idle Line State

The Line State Detector recognizes the incoming data to be in the Super Idle Line State upon the reception of 8 consecutive Idle symbol pairs nominally (plus 1 symbol pair).

The Super Idle Line State is used to insure synchronization of PCM signalling.

No Signal Detect

The Line State Detector recognizes the incoming data to be in the No Signal Detect state upon the deassertion of the Signal Detect signal or lack of internal clock detect from the Clock Recovery Module, and reception of 8 Quiet symbol pairs nominally. No Signal Detect indicates that the incoming link is inactive. This is the same as receiving Quiet Line State (QLS).

Master Line State

The Line State Detector recognizes the incoming data to be in the Master Line State upon the reception of eight consecutive Halt-Quiet symbol pairs nominally (plus up to 2 symbol pairs in start up cases).

The Master Line State is used in the handshaking sequence of the PHY Connection Management process.

Halt Line State

The Line State Detector recognizes the incoming data to be in the Halt Line State upon the reception of eight consecutive Halt symbol pairs nominally (plus up to 2 symbol pairs in start up cases).

The Halt Line State is used in the handshaking sequence of the PHY Connection Management process.

Quiet Line State

The Line State Detector recognizes the incoming data to be in the Quiet Line State upon the reception of eight consecutive Quiet symbol pairs nominally (plus up to 9 bits of 0 in start up cases).

The Quiet Line State is used in the handshaking sequence of the PHY Connection Management process.

Noise Line State

The Line State Detector recognizes the incoming data to be in the Noise Line State upon the reception of 16 noise symbol pairs without entering any known line state.

The Noise Line State indicates that data is not being received correctly.

Line State Unknown

The Line State Detector recognizes the incoming data to be in the Line State Unknown state upon the reception of 1 inconsistent symbol pair (i.e. data that is not expected). This may signify the beginning of a new line state.

Line State Unknown indicates that data is not being received correctly. If the condition persists the Noise Line State (NLS) may be entered.

ELASTICITY BUFFER

The Elasticity Buffer performs the function of a "variable depth" FIFO to compensate for phase and frequency clock skews between the Receive Clock (RXC±) and the Local Byte Clock (LBC).

Bit 5 (EBOU) of the Receive Condition Register B (RCRB) is set to 1 to indicate an error condition when the Elasticity Buffer cannot compensate for the clock skew.

The Elasticity Buffer will support a maximum clock skew of 50 ppm with a maximum packet length of 4500 bytes.

To make up for the accumulation of frequency disparity between the two clocks, the Elasticity Buffer will insert or delete Idle symbol pairs in the preamble. Data is written into the byte-wide registers of the Elasticity Buffer with the Receive Clock, while data is read from the registers with the Local Byte Clock.

The Elasticity Buffer will recenter (i.e. set the read and write pointers to a predetermined distance from each other) upon the detection of a JK or every four byte times during PHY Invalid (i.e. MLS, HLS, QLS, NLS, NSD) and Idle Line State. The Elasticity Buffer is designed such that a given register cannot be written and read simultaneously under normal operating conditions. To avoid metastability problems, the EB overflow event is flagged and the data is tagged before the over/under run actually occurs.

LINK ERROR DETECTOR

The Link Error Detector provides continuous monitoring of an active link (i.e. during Active and Idle Line States) to insure that it does not exceed the maximum Bit Error Rate requirement as set by the ANSI standard for a station to remain on the ring.

Upon detecting a link error, the internal 8-bit Link Error Monitor Counter is decremented. The start value for the Link Error Monitor Counter is programmed through the Link Error Threshold Register (LETR). When the Link Error Monitor Counter reaches zero, bit 4 (LEMT) of the Interrupt Condition Register (ICR) is set to 1. The current value of the Link Error Monitor Counter can be read through the Current Link Error Count Register (CLECR). For higher error rates the current value is an approximate count because the counter rolls over.

There are two ways to monitor Link Error Rate: polling and interrupt.

Polling

The Link Error Monitor Counter can be set to a large value, like FF. This will allow for the greatest time between polling the register. This start value is programmed through the Link Error Threshold Register (LETR).

Upon detecting a link error, the Line Error Monitor Counter is decremented.

The Host System reads the current value of the Link Error Monitor Counter via the Current Link Error Count Register (CLECR). The Counter is then reset to FF.

Interrupt

The Link Error Monitor Counter can be set to a small value, like 5 to 10. This start value is programmed through the Link Error Threshold Register (LETR).

Upon detecting a link error, the Line Error Monitor Counter is decremented. When the counter reaches zero, bit 4 (LEMT) of the Interrupt Condition Register (ICR) is set to 1, and the interrupt signal goes low, interrupting the Host System.

Miscellaneous Items

When bit 0 (RUN) of the Mode Register (MR) is set to zero, or when the PLAYER+ device is reset through the Reset pin (~RST), the internal signal detect line is internally forced to zero and the Line State Detector is set to Line State Unknown and No Signal Detect.

3.0 Functional Description (Continued)

3.3 TRANSMITTER BLOCK

The Transmitter Block accepts 10-bit bytes consisting of 8 bits data, 1 bit parity, and 1 bit control information, from the Configuration Switch.

The Transmitter Block performs the following operations:

- Encodes the data from 4B to 5B coding.
- Filters out code violations from the data stream.
- Is capable of generating Idle, Master, Halt, Quiet, or other user defined symbol pairs.
- Converts the data stream from NRZ to NRZI for transmission.
- Serializes data.

During normal operation, the Transmitter Block presents serial data to a PMD transmitter.

While in Internal Loopback mode, the Transmitter Block presents serial data to the Receiver Block. While in the External Loopback mode, the Transmitter Block presents serial data to the Clock Recovery Module.

The Transmitter Block consists of the following functional blocks:

Data Registers
Parity Checker
4B/5B Encoder
Repeat Filter
Smoother
Line State Generator
Injection Control Logic
Shift Register
NRZ to NRZI Encoder

See *Figure 3-3*, Transmitter Block Diagram.

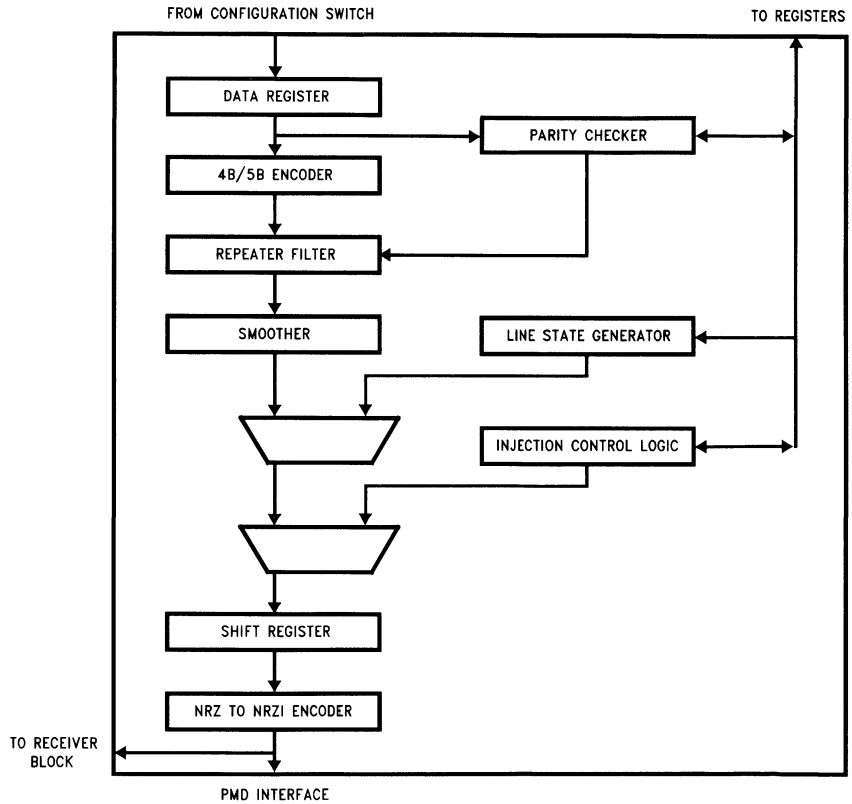

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FIGURE 3-3. Transmitter Block Diagram

3.0 Functional Description (Continued)

DATA REGISTERS

Data from the Configuration Switch is stored in the Data Registers. The 10-bit byte-wide data consists of a parity bit, a control bit, and two 4-bit data symbols as shown below.

b9	b8	b7 b0
Parity Bit	Control Bit	Data Bits

FIGURE 3-4. Byte-Wide Data

The parity is odd parity. The control bit determines whether the Data bits represent Data or Control information. When the control bit is 0 the Data field is interpreted as data and when it is 1 the field is interpreted as control information according to the National Semiconductor control codes.

PARITY CHECKER

The Parity Checker verifies that the parity bit in the Data Register represents odd parity (i.e. odd number of 1s).

The parity is enabled and disabled through bit 6 (PRDPE) of the Current Transmit State Register (CTSR).

If a parity error occurs, the Parity Checker will set bit 0 (DPE) in the Interrupt Condition Register (ICR) and report the error to the Repeat Filter.

4B/5B ENCODER

The 4B/5B Encoder converts the two 4-bit data symbols from the Configuration Switch into their respective 5-bit codes.

See Table 3-2 for the Symbol Encoding list.

TABLE 3-2. 4B/5B Symbol Encoding

Symbol	4B Code	5B Code
0	0000	11110
1	0001	01001
2	0010	10100
3	0011	10101
4	0100	01010
5	0101	01011
6	0110	01110
7	0111	01111
8	1000	10010
9	1001	10011
A	1010	10110
B	1011	10111
C	1100	11010
D	1101	11011
E	1110	11100
F	1111	11101
N	0000	11110 or 11111
JK (Starting Delimiter)	1101	11000 and 10001
T (Ending Delimiter)	0100 or 0101	01101
R (Reset)	0110	00111

Note: The upper group of symbols are sent with the Control/Data pin set to Data, while the bottom grouping of symbols are sent with the Control/Data pin set to Control.

REPEAT FILTER

The Repeat Filter is used to prevent the propagation of code violations to the downstream station.

Upon receiving violations in data frames, the Repeat Filter replaces them with two Halt symbol pairs followed by Idle symbols. Thus the code violations are isolated and recovered at each link and will not be propagated throughout the entire ring.

3.0 Functional Description (Continued)

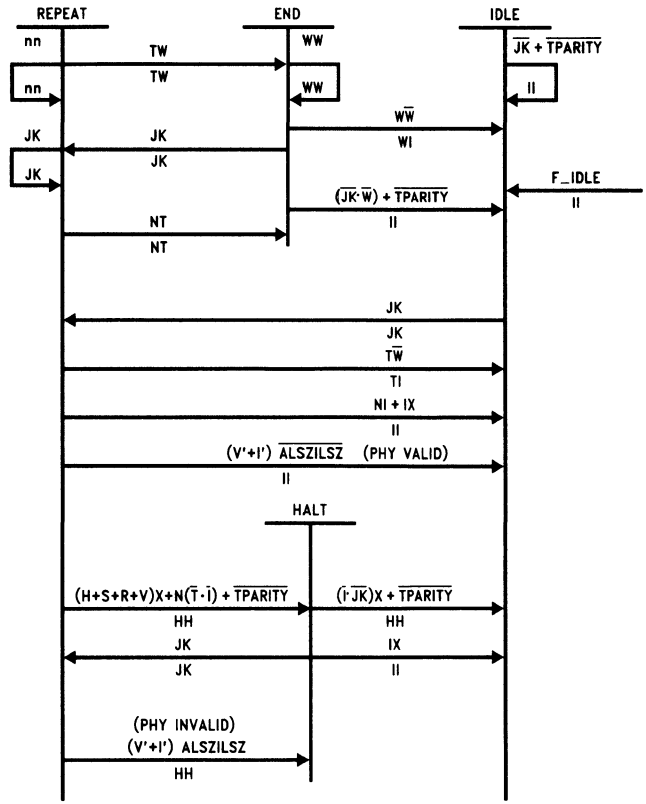

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FIGURE 3-5. Repeat Filter State Diagram

Note: Inputs to the Repeat Filter state machine are shown above the transition lines, while outputs from the state machine are shown below the transition lines.

Note: Abbreviations used in the Repeat Filter State Diagram are shown in Table 3-3.

TABLE 3-3. Abbreviations used in the Repeat Filter State Diagram

F_IDLE:	Force Idle_true when not in Active Transmit Mode.
W:	Represents the symbols R, or S, or T
~TPARITY:	Parity error
nn :	Data symbols (for C = 0 in the PHY-MAC interface)
N:	Data portion of a control and data symbol mixture
X:	Any symbol (i.e. don't care)
V':	Violation symbols or symbols inserted by the Receiver Block
I':	Idle symbols or symbols inserted by the Receiver Block
ALSZILSZ:	Active Line State or Idle Line State (i.e. PHY Invalid)
~ALSZILSZ:	Not in Active Line State nor in Idle Line State (i.e. PHY Valid)
H:	Halt Symbol
R:	Reset Symbol
S:	Set Symbol
T:	Frame ending delimiter
JK:	Frame start delimiter
I:	Idle symbol (Preamble)
V:	Code violations

The Repeat Filter complies with the FDDI standard by observing the following (see *Figure 3-5*):

1. In Repeat State, violations cause transitions to Halt State and two Halt symbol pairs are transmitted (unless JK or Ix occurs) followed by transition to Idle State.
2. When Ix is encountered, the Repeat Filter goes to the Idle State, during which Idle symbol pairs are transmitted until a JK is encountered.
3. The Repeat Filter goes to the Repeat State following a JK from any state.

The END State, which is not part of the FDDI PHY standard, allows an R or S prior to a T within a frame to be recognized as a violation. It also allows NT to end a frame as opposed to being treated as a violation.

SMOOTHER

The Smoother is used to keep the preamble length of a frame to a minimum of 6 Idle symbol pairs.

Idle symbols in the preamble of a frame may have been added or deleted by each station to compensate for the difference between the Receive Clock and its Local Clock. The preamble needs to be maintained at a minimum length to allow stations enough time to complete processing of one frame and prepare to receive another. Without the Smoother function, the minimum preamble length (6 Idle symbol pairs) cannot be maintained as several stations may consecutively delete Idle symbols.

The Smoother attempts to keep the number of Idle symbol pairs in the preamble at 7 by:

- Deleting an Idle symbol pair in preambles which have more than 7 Idle symbol pairs

and/or

- Inserting an idle symbol pair in preambles which have less than 7 idle symbol pairs (i.e. Extend State).

The Smoother Counter starts counting upon detecting an Idle symbol pair. It stops counting upon detecting a JK symbol pair.

Figure 3-6 describes the Smoother state diagram.

3.0 Functional Description (Continued)

LINE STATE GENERATOR

The Line State Generator allows the transmission of the PHY Request data and can also generate and transmit Idle, Master, Halt, or Quiet symbol pairs which can be used to implement the Connection Management procedures as specified in the FDDI Station Management (SMT) standard document.

The Line State Generator is programmed through Transmit bits 0 to 2 (TM<2:0>) of the Current Transmit State Register (CTSR).

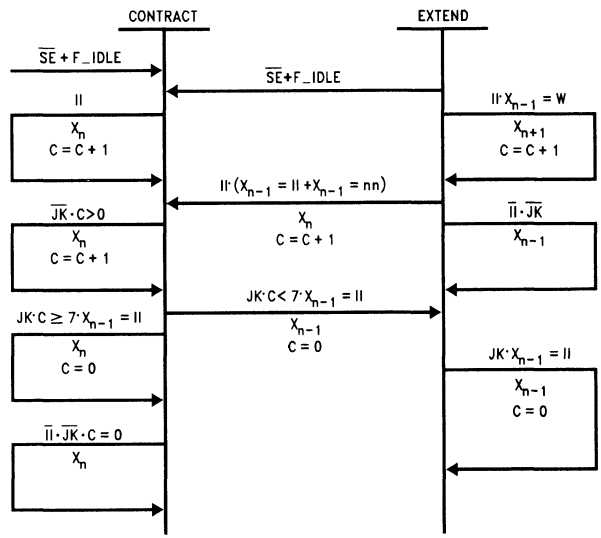
Based on the setting of these bits, the Transmitter Block operates in a Transmit Mode where the Line State Generator overwrites the Repeat Filter and Smoother outputs.

See INJECTION CONTROL LOGIC section for a listing of the injection Transmit Modes.

Table 3-4 describes the Transmit Modes.

TABLE 3-4. Transmit Modes

Transit Mode	Behavior
Active Transmit Mode	Transmit data that comes from Configuration Switch
Off Transmit Mode	Transmit Quiet symbol pairs and disable the PMD Transmitter
Idle Transmit Mode	Transmit Idle symbol pairs
Master Transmit Mode	Transmit Halt-Quiet symbol pairs
Quiet Transmit Mode	Transmit Quiet symbol pairs
Reserved Transmit Mode	Reserved for future use. If Mode selected, Quiet symbol pairs will be transmitted.
Halt Transmit Mode	Transmit Halt Symbol pairs



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Notes:

SE: Smoother Enable
C: Preamble Counter
F_IDLE: Force_Idle (Stop or $\overline{ATM}$)
X_n: Current Byte
X_{n-1}: Previous Byte
W: RST

FIGURE 3-6. Smoother State Diagram

3.0 Functional Description (Continued)

INJECTION CONTROL LOGIC

The Injection Control Logic replaces the data stream with a programmable symbol pair. This function is used to transmit data other than the normal data frame or Line States. The injection modes can be used for station diagnostic software.

The Injection Symbols overwrite the Line State Generator (Transmit Modes) and the Repeat Filter and Smoother outputs.

These programmable symbol pairs are stored in the Injection Symbol Register A (ISRA) and Injection Symbol Register B (ISRB). The Injection Threshold Register (IJTR) determines where the Injection Symbol pair will replace the data symbols.

The Injection Control Logic is programmed through the bits 0 and 1 (IC<1:0>) of the Current Transmit State Register (CTSR) to one of the following Injection Modes (see *Figure 3-7*):

1. No Injection (i.e. normal operation)
2. One Shot
3. Periodic
4. Continuous

In the No Injection mode, the data stream is transmitted unchanged.

In the One Shot mode, ISRA and ISRB are injected once on the nth byte after a JK, where n is the programmed value specified in the Injection Threshold Register.

In the Periodic mode, ISRA and ISRB are injected every nth symbol.

In the Continuous mode, all data symbols are replaced with the content of ISRA and ISRB. This is the same as periodic mode with IJTR = 0.

SHIFT REGISTER

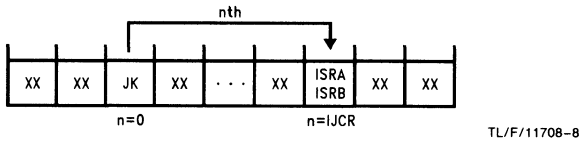
The Shift Register converts encoded parallel data to serial data. The parallel data is clocked into the Shift Register by the Local Byte Clock (LBC1), and clocked out by the Transmit Bit Clock (TXC±) (externally available on the DP83257.)

NRZ TO NRZI ENCODER

The NRZ to NRZI Encoder converts the serial Non-Return-To-Zero data to Non-Return-To-Zero-Invert-On-One format.

This function can be enabled and disabled through bit 6 (TNRZ) of the Mode Register (MR). When programmed to "0", it converts the bit stream from NRZ to NRZI. When programmed to "1", the bit stream is transmitted NRZ.

One Shot (Notes 1,3)



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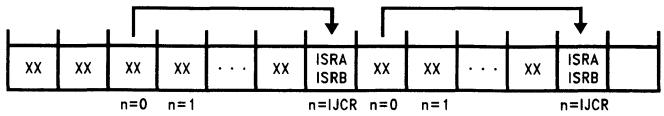
Periodic (Notes 2,3)



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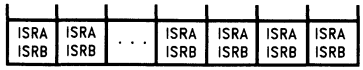
Continuous (Note 3)



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Note 1: In one shot, when n = 0, the JK is replaced

Note 2: In periodic, when n = 0, all symbols are replaced.

Note 3: Max value on n = 255.

FIGURE 3-7. Injection Modes

3.0 Functional Description (Continued)

3.4 CONFIGURATION SWITCH

The Configuration Switch consists of a set of multiplexers and latches which allow the PLAYER+ device to configure the data paths without any external logic. The Configuration Switch is controlled through the Configuration Register (CR).

The Configuration Switch has four internal buses: the A__Request bus, the B__Request bus, the Receive bus, and the PHY__Invalid bus. The two Request buses can be driven by external input data connected to the external PHY Port interface. The Receive bus is internally connected to the Receive Block of the PLAYER+ device, while the PHY__Invalid bus has a fixed 10-bit SMT PHY Invalid connection (LSU) pattern (1 0011 1010), which is useful during the connection process.

The configuration switch also has three internal multiplexers, each can select any of the four buses to connect to its respective data path. The first two are PHY Port interface output data paths, A__Indicate and B__Indicate, that can drive output data paths of the external PHY Port interface. The third output data path is connected internally to the Transmit Block.

The Configuration Switch is the same on both the DP83256 device and the DP83257 device. However, the DP83257 has two PHY Port interfaces connected to the Configuration Switch, whereas the DP83256 has one set of PHY port interfaces. The DP83257 uses the A__Request and A__Indicate paths as one PHY Port interface and the B__Request and B__Indicate paths as the other PHY Port interface (See *Figure 3-8*). The DP83256, having one port interface, uses the B__Request and A__Indicate paths as its external port. The A__Request and B__Indicate paths of the DP83256 are null connections and are not used by the device (See *Figure 3-9*).

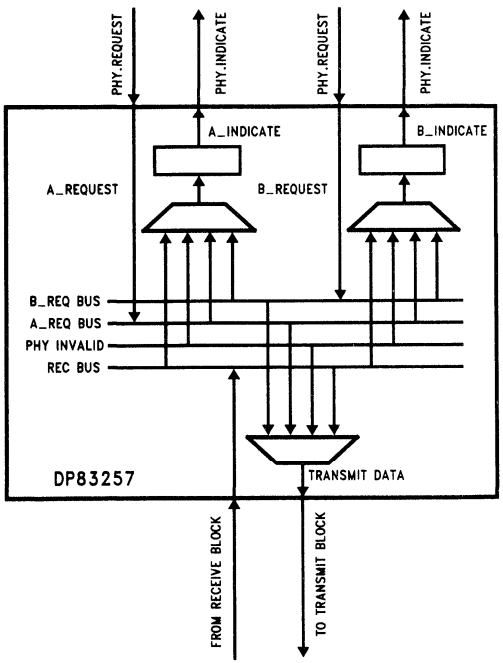

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FIGURE 3-8. Configuration Switch Block Diagram for DP83257

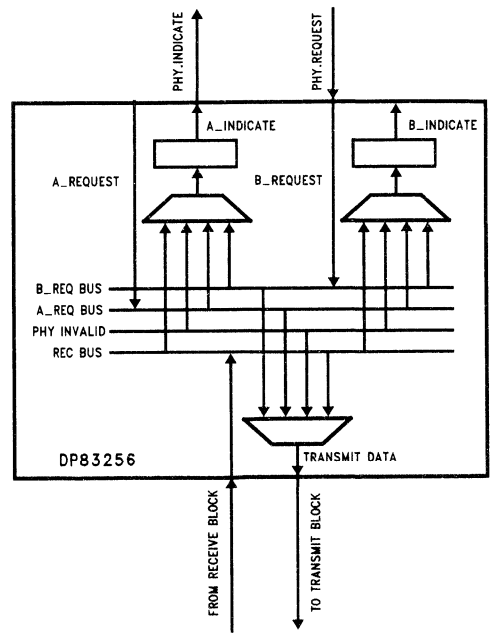

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FIGURE 3-9. Configuration Switch Block Diagram for DP83256

3.0 Functional Description (Continued)

STATION CONFIGURATIONS

Single Attach Station (SAS)

The Single Attach Station can be connected to either the Primary or Secondary ring via a Concentrator. Only 1 MAC is needed in a SAS.

Both the DP83256 and DP83257 can be used in a Single Attach Station. The DP83256 can be connected to the MAC via its only PHY Port interface. The DP83257 can be connected to the MAC via either one of its 2 PHY Port Interfaces.

See *Figure 3-10* and *Figure 3-11*.

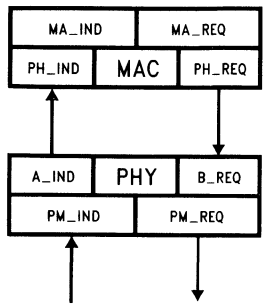

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FIGURE 3-10. Single Attach Station Using the DP83256

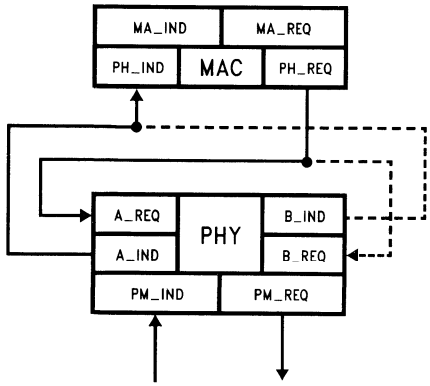

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FIGURE 3-11. Single Attachment Station (SAS) Using the DP83257

Dual Attach Station(DAS)

A Dual Attach Station can be connected directly to the dual ring, or, optionally to a concentrator. There are two types of Dual Attach Stations: DAS with a single MAC and DAS with two MAC layers. See *Figure 3-12* and *Figure 3-13*.

Two DP83256 parts can be connected together to build a Dual Attach Station, however this configuration does not support the optional Thru_B configuration. When the optional Thru_B configuration is desired, it is recommended that the DP83257 be used.

A DAS with a single MAC and two paths can be configured as follows (see *Figure 3-12*):

- B Indicate data of PHY_A is connected to A Request input of PHY_B. B_Request input of PHY_A is connected to A Indicate output of PHY_B.
- The MAC can be connected to either the A Request input and the A Indicate output of PHY_A or the B Request input and the B Indicate output of PHY_B.

A DAS with a single MAC and one path using the DP83256 can be configured as follows (see *Figure 3-13*):

- B_Request input of PHY_A is connected to A Indicate output of PHY_B.
- The MAC is connected to the B Request input of PHY_B and the A_Indicate output of PHY_A.

A DAS with dual MACs can be configured as follows (see *Figure 3-14*):

- B Indicate data of PHY_A is connected to A Request input of PHY_B. B_Request input of PHY_A is connected to A Indicate output of PHY_B.
- MAC_1 is connected to the B_Indicate output and the B_Request Input of PHY_B.
- MAC_2 is connected to the A_Indicate output and the A_Request Input of PHY_A.

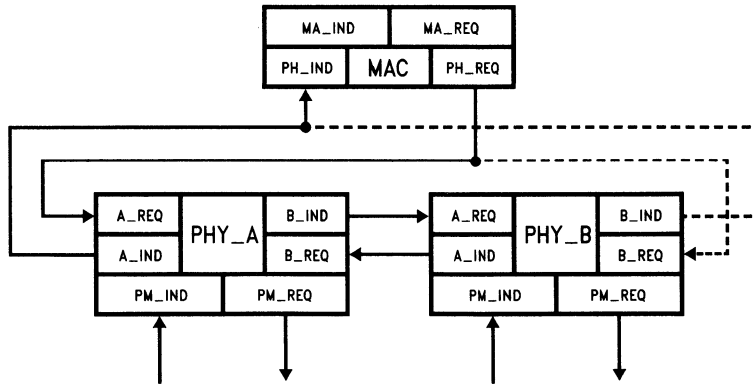

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FIGURE 3-12. Dual Attachment Station (DAS), Single MAC (DP83257)

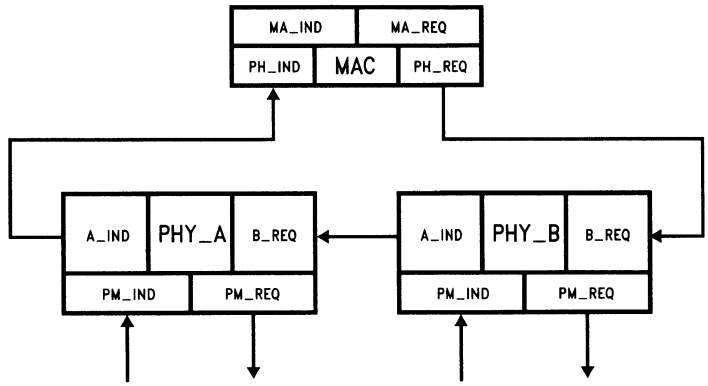

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FIGURE 3-13. Dual Attachment Station (DAS), Single MAC (DP83256)

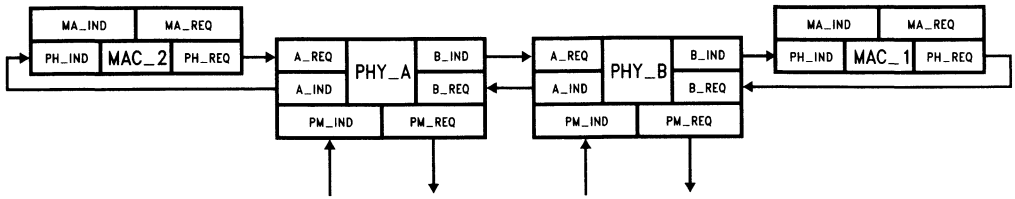

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FIGURE 3-14. Dual Attachment Station (DAS), Dual MACs

3.0 Functional Description (Continued)

CONCENTRATOR CONFIGURATIONS

There are 2 types of concentrators: Single Attach and Dual Attach. These concentrators can be designed with or without MAC(s). The configuration is determined based upon its type and the number of active MACs in the concentrator.

Using the PLAYER+ device, a concentrator can be built with many different configurations without any external logic.

Both the DP83256 and DP83257 can be used to build a Single Attach concentrator.

See Application Note AN-675, Designing FDDI concentrators and Application Note AN-741, Differentiating FDDI concentrators for further information.

Concepts

A concentrator is comprised of 2 parts: the Dual Ring Connect portion and the Master Ports.

The Dual Ring Connection portion connects the concentrator to the dual ring directly or to another concentrator. If the concentrator is connected directly to the dual ring, it is a part of the "Dual Ring of Trees". If the concentrator is connected to another concentrator, it is a "Branch" of the "Dual Ring of Trees".

The Master Ports connect the concentrator to its "Slaves", or S-class, Single Attach connections. A slave could be a Single Attach Station or another concentrator (thus forming another Branch of the Dual Ring Tree).

When a MAC in a concentrator is connected to the primary or secondary ring, it is required to be situated at the exit port of that ring (i.e. its PH_IND is connected to the IND Interface of the last Master Port in the concentrator (PHY_M n) that is connected to that ring).

A concentrator can have two MACs, one connected to the primary ring and one to the secondary ring. In addition, roving MACs can be included in the concentrator configuration. A roving MAC can be used to test the stations connected to the concentrator before allowing them to join the dual ring. This may require external multiplexers, if used in conjunction with two other MAC layers.

Single Attach Concentrator

A Single Attach concentrator is a concentrator that has only one PHY at the dual ring connect side. It cannot, therefore, be connected directly to the dual ring. A Single Attach concentrator is a branch to the dual ring tree. It is connected to the ring as a slave of another concentrator.

Multiple Single Attach concentrators can be connected together hierarchically to build a multiple levels of branches in a dual ring.

The Single Attach concentrator can be connected to either the primary or secondary ring depending on the connection with its concentrator (the concentrator that it is connected to as a slave).

Figure 3-15 shows a Single Attach concentrator with a single MAC.

Dual Attach Concentrator

A Dual Attach concentrator is a concentrator that has two PHYs on the dual ring connect side. It is connected directly to the dual ring and is a part of the dual ring tree.

The Dual Attach concentrator is connected to both the primary and secondary rings.

Dual Attach Concentrator with Single MAC

Figure 3-16 shows a Dual Attach concentrator with a single MAC.

Because the concentrator has one MAC, it can only transmit and receive frames on the ring to which the MAC is connected. The concentrator can only repeat frames on the other ring.

Dual Attach Concentrator with Dual MACs

Figure 3-17 shows a Dual Attach concentrator with dual MACs.

Because the concentrator has two MACs, it can transmit and receive frames on both the primary and secondary rings.

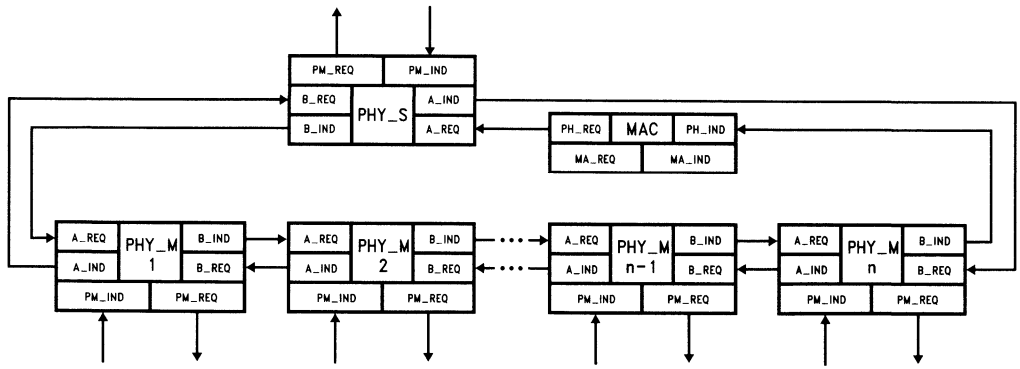

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FIGURE 3-15. Single Attach Concentrator (SAC), Single MAC

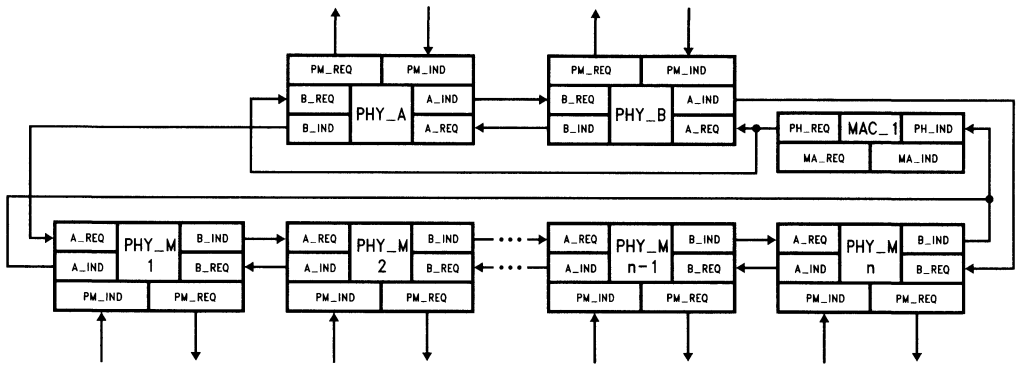

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FIGURE 3-16. Dual Attach Concentrator (DAC), Single MAC

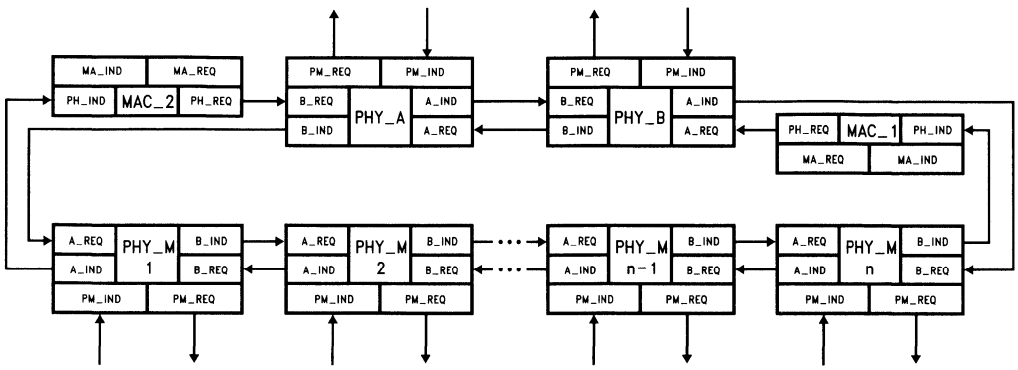

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FIGURE 3-17. Dual Attach Concentrator (DAC), Dual MACs

3.0 Functional Description (Continued)

3.5 CLOCK GENERATION MODULE

The Clock Generation Module is an integrated phase locked loop that generates all of the required clock signals for the PLAYER+ device and the rest of an FDDI system from a single 12.5 MHz reference.

The Clock Generation Module features:

- High precision clock timing generated from a single 12.5 MHz reference.
- Multiple precision phased (8 ns/16 ns) 12.5 MHz Local Byte Clocks to eliminate timing skew in large multi-board concentrator configurations.
- LBC timing which is insensitive to loading variations over a wide range (20 pF to 70 pF) of LBC loads.
- A selectable dual frequency system clock.
- Low clock edge jitter, due to high VCO stability.

The Clock Generation Module is comprised of 6 main functional blocks:

Reference Selector
Phase Comparator
Loop Filter
250 MHz Voltage Controlled Oscillator
Output Phasing and Divide by 10

See *Figure 3-18*, Clock Generation Module Block Diagram.

REFERENCE SELECTOR

The Reference Selector block allows the user to choose between 2 sources for the Clock Generation Module's 12.5 MHz reference clock.

The first reference clock source option is a local 12.5 MHz crystal circuit. The circuit consists of a single 12.5 MHz crystal connected between XTAL_IN and XTAL_OUT and 2 loading capacitors, one connected between XTAL_IN and Ground, and the other connected between XTAL_OUT and Ground. The circuit is shown in *Figure 3-19*.

The second reference clock source option is an external 12.5 MHz reference signal fed into the REF_IN input. This signal would typically be a Local Byte Clock generated by another PLAYER+ device. This allows one PLAYER+ device to create a master clock to which other PLAYER+ devices in a system can be synchronized to.

The REF_SEL signal selects between the two references.

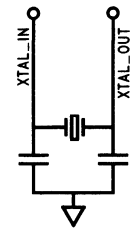

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FIGURE 3-19. Crystal Circuit

PHASE COMPARATOR

The Phase Comparator uses two signal inputs: the selected 12.5 MHz reference from the Reference Select Block and a Local Byte Clock that has been selected for the feedback input, FBK_IN.

The Phase Comparator generates a pulse of current that is proportional to the phase difference between the two signals. The current pulses are used to charge and discharge a control voltage on the internal Loop Filter. This control voltage is used to minimize the phase difference between the two signals.

LOOP FILTER

The Loop Filter is a simple internal filter made up of one capacitor in parallel with a serial capacitor and resistor combination. One end of the filter is connected to Ground and the other node is driven by the Phase Comparator and controls the internal 250 MHz Voltage Controlled Oscillator. This node can be examined on the LPFLTR pin when the FLTREN bit of the CGMREG register is enabled. The LPFLTR pin is provided for diagnostic purposes only and should not be connected in any application.

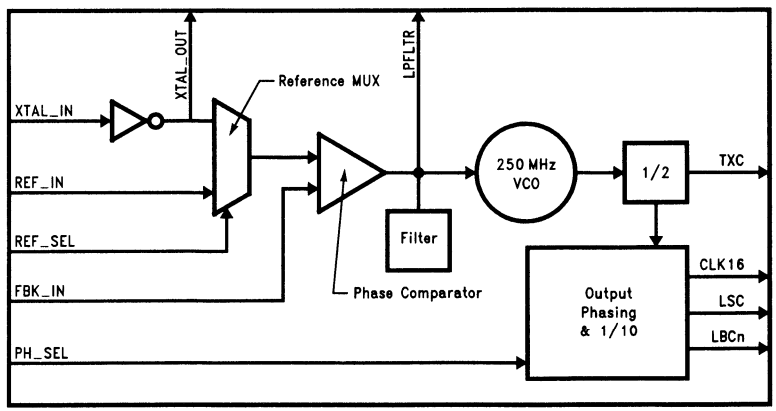

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FIGURE 3-18. Clock Generation Module Block Diagram

3.0 Functional Description (Continued)

The voltage on the Loop Filter is set by the current pulses generated by the Phase Comparator. The voltage on the Loop Filter node controls the frequency of the 250 MHz VCO.

250 MHZ VOLTAGE CONTROLLED OSCILLATOR (VCO)

The internal Voltage Controlled Oscillator is a low gain VCO whose primary frequency of oscillation centers around 250 MHz. The VCO produces little clock jitter due to its exceptional stability under all circumstances.

The VCO's output frequency is proportional to the voltage on the Loop Filter node.

OUTPUT PHASING

The Output Phasing block is a precision clock division circuit that produces clock signals of 4 distinct frequencies. Within the 12.5 MHz frequency, 5 clock signals with selectable 8 ns or 16 ns phase difference are produced.

The following clock signals are produced:

System Clock (CLK16/CLK32)
Local Symbol Clock (LSC)
Local Byte Clocks 1–5 (LBCn) (Divide by 10)

System Clock (CLK16/CLK32)

The System Clock is provided as an extra set of clock frequencies that may be used as a clock for non-FDDI chipset portions of a system or as a higher frequency System Interface clock for the MACSI device. This clock is derived by dividing the 125 MHz clock by 8 or 4 times.

The frequency is selectable through the CLKSEL bit of the MODE2 register. The output has built-in glitch suppression so that changing the CLKSEL bit will not result in glitches appearing at the output.

Local Symbol Clock (LSC)

The Local Symbol Clock is a 40% HIGH/60% LOW duty cycle clock provided for use by the MACSI device and any external logic that needs to be synchronized to the Symbol timing.

This clock is derived by dividing the 125 MHz clock by 5.

Local Byte Clocks 1–5 (LBCn)

The Local Byte Clocks are provided for use by the MACSI device, by any external logic that needs to be synchronized to the Byte timing, and for use in concentrators to synchronize the timing between multiple PLAYER+ devices.

These clocks are derived by dividing the 125 MHz clock by 10. The different phase relationships between the LBCs are achieved by tapping off of different outputs of a Johnson counter inside the Output Phasing block.

The phase relationship (separation by 8 ns or 16 ns) of the LBCs is selected using the PH_SEL pin.

One of the LBCs must be used as the source of the feedback input, FBK_IN, which requires a 12.5 MHz frequency. When the PLAYER+ device is using a crystal as a reference it does not matter which LBC is used as the feedback input. Typically the least loaded LBC is used. However, when using an external reference that is supplied by another PLAYER+ device, it is important to select the LBC that keeps your system properly synchronized.

3.6 STATION MANAGEMENT SUPPORT

The Station Management Support Block provides a number of useful features to simplify the implementation of the Connection Management (CMT) portion of SMT.

These features eliminate the most severe CMT response time constraints imposed by the PC_React and CF_React times. The many integrated counters and timers also eliminate the need for additional external devices.

The following CMT features are supported:

- PC_React
- CF_React
- Auto Scrubbing (TCF Timer)
- Timer, Idle Detection (TID Timer)
- Noise Event Counter (TNE Timer)
- Link Error Monitor (LEM Counter)

PC_REACT

PC_React is one of the timing restrictions imposed by Connection Management (CMT). It is one of the two most critical timing restrictions imposed (the other being CF_React.)

The ANSI SMT standard states that "PC_React is the maximum time for PCM [Physical Connection Management] to make a state transition to PC_Break when QLS, a fault condition, or PC_Start signal is present. This maximum time also places a limit on the time to react to a PC_Stop signal. This limitation does not apply to any other PCM transitions." PC_React puts a sharp time limit on how long it takes to transition to the PC_Break state and transmit the correct line state when a PC_Break transition is required.

The range for the timer is PC_React $\leq$ 3.0 ms and has a default value equal to 3.0 ms.

The PLAYER+ device contains a Trigger Definition Register and a set of CMT Condition Registers that can be used to satisfy the PC_React timing.

The Trigger Definition Register (TDR) controls two functions. First, it allows the selection of the line state(s) on which to trigger (SILS, MLS, HLS . . .). For PC_React, the line states used would be the ones that caused a transition to the PC_Break state from the current PCM state.

Second, it allows specification of a line state to be transmitted when the trigger condition is met. For PC_React, this is the line state that needs to be transmitted when a transition to the PC_Break state occurs, which is Quiet Line State (QLS).

The set of CMT Condition registers controls interrupt generation when a trigger condition occurs. The CMT Condition Register set includes a CMT Condition Register (CMTCR), a CMT Condition Comparison Register (CMTCCR), and a CMT Condition Mask Register (CMTCMR).

Line state triggering for PC_React is enabled by selecting line states to trigger on from the Trigger Definition Register (TDR) bits 3-7.

The Trigger Condition Occurred (TCO) bit of the CMTCR is automatically set when the trigger condition specified by the TDR register is met.

The line state specified by the Trigger Definition Register (TDR) bits 0–2 is then loaded into the Current Transmit Mode Register (CTSR), causing the line state to be transmitted.

3.0 Functional Description (Continued)

If the TCO Mask (TCOM) bit of the CMTCMR is set, then whenever the CMTCR.TCO bit becomes set the Receive Condition Register B's Connection Service Event (RCRB.CSE) bit will be set. This allows an interrupt to be generated for the trigger event.

As an example, suppose the PCM state machine is in the ACTIVE state. From this state, if a Halt Line State (HLS) or Quiet Line State (QLS) is detected, or the Noise Threshold is reached, the state machine must move to the PC__Break state and begin transmitting QLS. To implement this behavior when the PC__ACTIVE state is entered, set TDR.TTM2-0 to 110 (Quiet Transmit), set TDR.TOHLS, TDR.TOQLS, and TDR.TONT and reset all other bits (TOSILS and TOMLS). Also set CMTCMR.TCOM if an interrupt is desired.

CF__REACT

CF__React is one of the timing restrictions imposed by Connection Management (CMT). It is one of the two most critical timing restrictions imposed (the other being PC__React).

The ANSI SMT standard states that "CF__React is the maximum time for CFM [Configuration Management] to reconfigure to remove a non-Active connection from the token path."

The range for the timer is CF__React $\leq$ 3.0 ms and has a default value equal to 3.0 ms.

The PLAYER+ device contains a Trigger Transition Configuration Register and a set of CMT Condition Registers that can be used to satisfy the CF__React timing.

he Trigger Transition Configuration Register (TTCR) holds the new configuration switch settings to be loaded into the Configuration Register (CR) when a trigger condition occurs.

Enabling line state triggering with the Trigger Definition Register (TDR) bits 3-7 also enables the CF__React response. This means that whenever trigger conditions are actively used for PC__React, the value of the TTCR register will be used also. This implies that it either must always then be loaded with the current configuration setting, causing no change to the CR, or it must be loaded with the appropriate value to accommodate the CF__React function.

The Trigger Transition Configuration Register (TTCR) must be set the configuration desired when the trigger condition occurs. When the trigger condition occurs the value of this register is loaded into the Configuration Register (CR). During this time writes to the CR are inhibited.

To continue the example from the PC__React description, suppose that when in the ACTIVE state for the PCM state machine, the CFM state machine is also in the THRU__A state. If trigger conditions are enabled via the CMTCMR.TCOM bit and it is desired to not implement CF__React, TTCR must be set to the present value of CR. If it is desired to not implement CF__React then TTCR should be set to the value which would change the configuration to the WRAP state. The wrap conditions WRAP__A or WRAP__B depend on which PHY gets reconfigured.

AUTO SCRUBBING

Auto Scrubbing is an additional CMT feature that further enhances the automatic configuration switch setting in order to meet the CF__React timing. When enabled, Auto Scrubbing causes 2 PHY__Invalid symbols followed by Scrub Symbol pairs (Idles) to be sourced for a user selectable duration (the scrubbing time) after a trigger condition (the same one used for PC__React and CF__React) occurs and prior to a change in the configuration switch setting on all indicate ports that will be changed.

Auto Scrubbing is enabled by setting the Enable Scrubbing on Trigger Conditions (ESTC) bit of Mode Register 2 (MODE2).

The Scrub Timer Threshold Register (STTR) defines the duration of the scrubbing, which can last up to approximately 10ms. The Scrub Timer Value Register (STVR) can be used to examine a snapshot of the upper 8 bits of the STTR register.

TIMER, IDLE DETECTION

The Idle Detection Timer is required to flag the continued presence of the Idle Line State for a duration of 8 Idle Symbol pairs plus 1 symbol pair.

This feature is implemented in the Receiver Block by the Super Idle Line State (SILS).

NOISE EVENT COUNTER

The Noise Event Counter can be used to time the duration between Noise Events (which are described in detail below) and to count frame sizes. The first feature is the most often recognized, but the second is often overlooked and can lead to potential difficulty if not properly set.

The Noise Event Counter is implemented as a pair of down counters: one the actual Noise Counter and the other a Noise Counter Prescaling value. The Noise Threshold Register (NTR) and the Noise Prescale Threshold Register (NPTR) can be programmed to the counter's initial value while the Current Noise Count Register (CNCR) and the Current Noise Prescale Count Register (CNPCR) provide a snapshot of the actual counter.

The Noise Event Counter decrements whenever a Noise Line State (NLS), Line State Unknown (LSU), or Active Line State (ALS) is received and has its start value reloaded whenever it receives Halt Line State (HLS), Idle Line State (ILS), Master Line State (MLS), Quiet Line State (QLS), or No Signal Detect (NSD). The Noise Event Counter is also reset for a Start or End Delimiter. This means the Noise counter increments for bad events as well as for every data symbol in a frame. Should the Noise Counter expire, it indicates that a new line state (including ALS) has not been entered for NT__MAX time. This indicates that either a frame is too long or that noise is being received.

For this reason it is important to choose a value for the counter that is larger than the longest frame of 4500 bytes. The ANSI SMT specification recommends a value for NT__MAX of 1.3ms for the noise threshold.

A Noise Event is defined as follows:

A noise event is a noisebyte, or a byte of data which is not in line with the current line state, indicating error or corruption.

TABLE 3-5. Noise Event Description

Noise Event =	[SD • ~CD] + [SD • CD • PI • ~(II + JK + AB)] + [SD • CD • ~PI • (PB = II) • AB]
Where:	
•	= Logical AND
+	= Logical OR
~	= Logical NOT
SD	= Signal Detect
CD	= Clock Detect
PB	= Previous Byte
PLS	= Previous Line State
PI	= PHY Invalid = HLS + QLS + MLS + NLS + {ULS • [PLS = (ALS + ILS)]}
ILS	= Idle Line State
ALS	= Active Line State
ULS	= Unknown Line State
HLS	= Halt Line State
QLS	= Quiet Line State
MLS	= Master Line State
NLS	= Noise Line State
ULS	= Unknown Line State
I	= Idle symbol
J	= First symbol of start delimiter
K	= Second symbol of start delimiter
R	= Reset symbol
S	= Set symbol
T	= End Delimiter
A	= n + R + S + T
B	= n + R + S + T + I
n	= any data symbol

LINK ERROR MONITOR

Link Error Monitoring is accomplished in the PLAYER+ device through the Link Error Monitor Counter. The initial value of this down counter is set using the Link Error Threshold Register (LETR). A snapshot of the counter can be taken with the Current Link Error Count Register (CLECR).

A Link Error is defined as follows:

TABLE 3-6. Link Error Event Description

Link Error Event =	[ALS • (I~I + xV + Vx + H~H)] + [ALS • ~SD] + [ILS • ~(II + JK)] + [ILS • ~SD)] + [ULS • (PLS=ALS) • Link_Error_Flag • ~SB • ~(HH + HI + II + JK)]
Set Link_Error_Flag =	[ALS • (HH + NH + RH + SH + TH)]
Clear Link_Error_Flag =	[ALS • JK] + [ILS • JK] + [ULS • (PLS=ALS • Link_Error_Flag • ~SB • ~(HH + HI + II + JK)]
Where:	
~	= Logical NOT
+	= Logical OR
•	= Logical AND
ILS	= Idle Line State
ALS	= Active Line State
ULS	= Unknown Line State
x	= Any symbol
I	= Idle symbol
H	= Halt symbol
J	= First symbol of start delimiter
K	= Second symbol of start delimiter
V	= Violation symbol
R	= Reset symbol
S	= Set symbol
T	= End delimiter symbol
N	= Data symbol converted to 0000 by the PLAYER+ device Receiver Block in symbol pairs that contain a data and a control symbol
PLS	= Previous Line State
SD	= Signal Detect
SB	= Stuff Byte: Byte inserted by EB before a JK symbol pair for recentering or due to off-axis JK

3.0 Functional Description (Continued)

3.7 PHY-MAC INTERFACE

NATIONAL BYTE-WIDE CODE

The PLAYER+ device outputs the National byte-wide code from its PHY Port Indicate Output to the MAC device. Each National byte-wide code may contain data or control codes or the line state information of the connection. Table 3-7 lists all the possible outputs.

During Active Line State all data and control symbols are being repeated to the PHY Port Indicate Output with the exception of data in data-control mixture bytes. That data symbol is replaced by zero. If only one symbol in a byte is a control symbol, the data symbol will be replaced by 0000 and the whole byte will be presented as control code. Note that the Line State Detector recognizes the incoming data to be in the Active Line State upon reception of the Starting Delimiter (JK symbol pair).

During Idle Line State any non Idle symbols will be reflected as the code I'uILS. If both symbols received during Idle Line State are Idle symbols, then the Symbol Decoder generates I'kILS as its output. Note the coded Known/Unknown Bit (b3) and the Last Known Line State (b2–0). The Receive State is 4 bits long and it represents either the PHY Invalid (0011) or the Idle Line State (1011) condition. The Known/Unknown Bit shows if the symbols received match the line state information in the last 3 bits.

During any line state other than Idle Line State or Active Line State, the Symbol Decoder generates the code V'kLS if the incoming symbols match the current line state. The symbol decoder generates V'uLS if the incoming symbols do not match the current line state.

TABLE 3-7. National Byte Wide Code

Current Line State	Symbol 1		Symbol 2		National Code	
	Control Bit	Data	Control Bit	Data	Control Bit	Data
ALS	0	n	0	n	0	n-n
ALS	0	n	1	C	1	N-C
ALS	1	C	0	n	1	C-N
ALS	1	C	1	C	1	C-C
ILS	1	I	1	I	1	I'-k-LS
ILS	1	I	x	Not I	1	I'-u-LS
ILS	x	Not I	1	I	1	I'-u-LS
ILS	x	Not I	x	Not I	1	I'-u-LS
Stuff Byte during ILS	x	x	x	x	1	I'-k-ILS
Not ALS and Not ILS	1	M	1	M	1	V'-k-LS
Not ALS and Not ILS	1	M	x	Not M	1	V'-u-LS
Not ALS and Not ILS	x	Not M	1	M	1	V'-u-LS
Not ALS and Not ILS	x	Not M	x	Not M	1	V'-u-LS
Stuff Byte during Not ALS	x	x	x	x	1	V'-k-LS, V'-u-LS or L'-u-ILS
EB Overflow/Underflow					1	0011 1011
SMT_PI Connection (LSU)					1	0011 1010
Scrub Symbol Pair					1	1011 1000

Where:

n = Any data symbol in {0, 1, 2 . . . F}
C = Any control symbol in {V, R, S, T, I, H}
N = 0000 = Code for data symbol in a data control mixture byte
I = Idle Symbol
M = Any symbol that matches the current line state
I' = 1011 = First symbols of the byte in Idle Line State
V' = 0011 = PHY Invalid
LS = Line State
- ALS = 000
- ILS = 001
- NSD = 010
- MLS = 100
- HLS = 101
- QLS = 110
- NLS = 111

u = 1 = Indicates symbol received does not match current line state
k = 0 = Indicate symbol received matches current line state
x = Don't care

3.0 Functional Description (Continued)

National Byte-Wide Code Example

Incoming 5B Code			**Decoded 4B Code**					**National Byte-Wide Code (w/o parity)**			
98765	**43210**		**C**	**3210**	**C**	**3210**		**C**	**7654**	**3210**	
11111	11111	(II)	1	1010	1	1010	(II)	1	1011	0001	(I′-k-ILS)*
11111	11111	(II)	1	1010	1	1010	(II)	1	1011	0001	(I′-k-ILS)
11111	11111	(II)	1	1010	1	1010	(II)	1	1011	0001	(I′-k-ILS)
11000	10001	(JK)	1	1101	1	1102	(JK)	1	1101	1101	(JK Symbols)
—	—	(xx)	0	—	0	—	(xx)	0	—	—	(Data Symbols)
—	—	(xx)	0	—	0	—	(xx)	0	—	—	(Data Symbols)
—	—	(xx)	0	—	0	—	(xx)	0	—	—	(Data Symbols)
(More data __)											
—	—	(xx)	0	—	0	—	(xx)	0	—	—	(Data Symbols)
—	—	(xx)	0	—	0	—	(xx)	0	—	—	(Data Symbols)
—	—	(xx)	0	—	0	—	(xx)	0	—	—	(Data Symbols)
01101	00111	(TR)	1	0101	1	0110	(TR)	1	0101	0110	(T and R Symbols)
00111	00111	(RR)	1	0110	1	0110	(RR)	1	0110	0110	(Two R Symbols)
11111	11111	(II)	1	1010	1	1010	(II)	1	1010	1010	(Idle Symbols)
11111	11111	(II)	1	1010	1	1010	(II)	1	1010	1010	(Idle Symbols)
11111	11111	(II)	1	1010	1	1010	(II)	1	1011	0001	(I′-k-ILS)
11111	11111	(II)	1	1010	1	1010	(II)	1	1011	0001	(I′-k-ILS)
11111	11111	(II)	1	1010	1	1010	(II)	1	1011	0001	(I′-k-ILS)
00100	00100	(HH)	1	0001	1	0001	(HH)	1	1011	1001	(I′-u-ILS)
00100	00100	(HH)	1	0001	1	0001	(HH)	1	1011	1001	(I′-u-ILS)
00100	00100	(HH)	1	0001	1	0001	(HH)	1	1011	1001	(I′-u-ILS)
00100	00100	(HH)	1	0001	1	0001	(HH)	1	1011	1001	(I′-u-ILS)
00100	00100	(HH)	1	0001	1	0001	(HH)	1	1011	1001	(I′-u-ILS)
00100	00100	(HH)	1	0001	1	0001	(HH)	1	1011	1001	(I′-u-ILS)
00100	00100	(HH)	1	0001	1	0001	(HH)	1	1011	1001	(I′-u-ILS)
00100	00100	(HH)	1	0001	1	0001	(HH)	1	0011	0101	(V′-k-HLS)
00100	00100	(HH)	1	0001	1	0001	(HH)	1	0011	0101	(V′-k-HLS)
00100	00100	(HH)	1	0001	1	0001	(HH)	1	0011	0101	(V′-k-HLS)
11111	11111	(II)	1	1010	1	1010	(II)	1	0011	1101	(V′-u-HLS)
11111	11111	(II)	1	1010	1	1010	(II)	1	1011	0001	(I′-k-ILS)
11111	11111	(II)	1	1010	1	1010	(II)	1	1011	0001	(I′-k-ILS)

*Assume the receiver is in the Idle Line State.

3.0 Functional Description (Continued)

3.8 PMD INTERFACE

The PMD Interface connects the PLAYER+ device to a standard FDDI Physical Media Connection such as a fiber optic transceiver or a copper twisted pair transceiver. It is a 125 MHz full duplex serial connection.

The DP83256 PLAYER+ device contains one PMD interface. This PMD Interface should be used for all PMD implementations that do not require an external scrambler/descrambler function, clock recovery function, or clock generation function, such as a Fiber Optic or Shielded Twisted Pair (SDDI) PMDs.

The DP83257 PLAYER+ device contains two PMD interfaces. The PMD Interface should be used for all PMD implementations that do not require an external scrambler/descrambler function, clock recovery function, or clock generation function, such as a Fiber Optic or Shielded Twisted Pair (SDDI) PMDs. The second, Alternate PMD Interface can be used to support Unshielded Twisted Pair (UTP) PMDs that require external scrambling, and allows implementation with no external clock recovery or clock generation functions required.

PLAYER+ TO PMD CONNECTIONS

The following figures illustrate how the PLAYER+ device can be connected to various types of PMDs.

Figure 3-20 shows how the DP83256 or DP83257 PLAYER+ device is connected to a Fiber Optic or Shielded Twisted Pair (SDDI) PMD using the Primary PMD Interface.

Figure 3-21 shows how the DP83257 PLAYER+ device is connected to an Unshielded Twisted Pair (UTP) PMD using the Alternate PMD Interface.

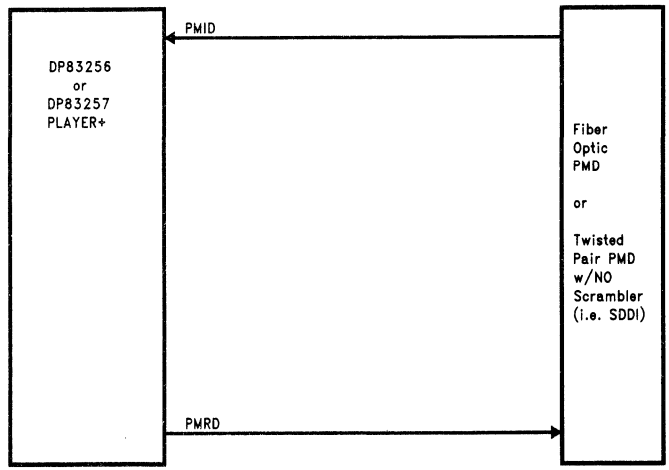

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FIGURE 3-20. Fiber Optic or STP PMD Connection

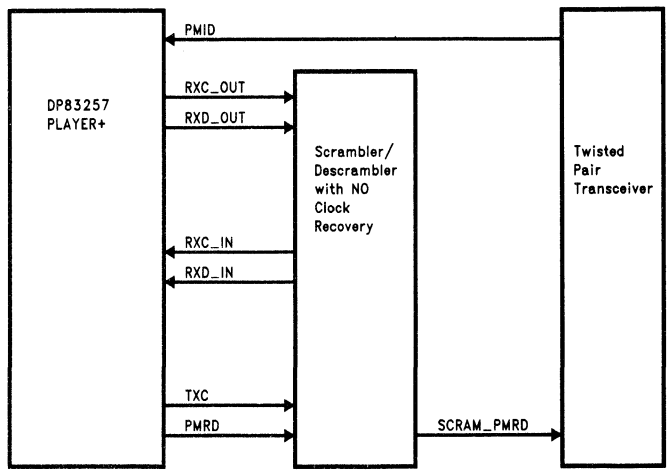

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FIGURE 3-21. UTP PMD Connections

Figure 3-22 shows one way that a PMD using an external scrambler/descrambler and an external clock recovery device could be used with the DP83257 PLAYER+ device, bypassing the PLAYER+ device's built in Clock Recovery Module (CRM).

INTERFACE ACTIVATION

The Primary PMD Interface is always enabled.

The Alternate PMD Interface is enabled by programming a PLAYER+ register bit. To enable the interface, write a 1 to the APMDEN bit in the APMDREG register. The interface is off by default and should be left that way unless it is being used.

It will also probably be necessary to enable the Transmit Clocks when using the Alternate PMD Interface. The Transmit Clocks (TXC) are enabled by writing a 1 to the TXCE bit in the CGMREG register. The transmit clocks are disabled by default and should be left that way unless it is being used.

Note that when the Alternate PMD Interface is active, the Primary PMD Interface can not be used without the Alternate PMD Interface connections.

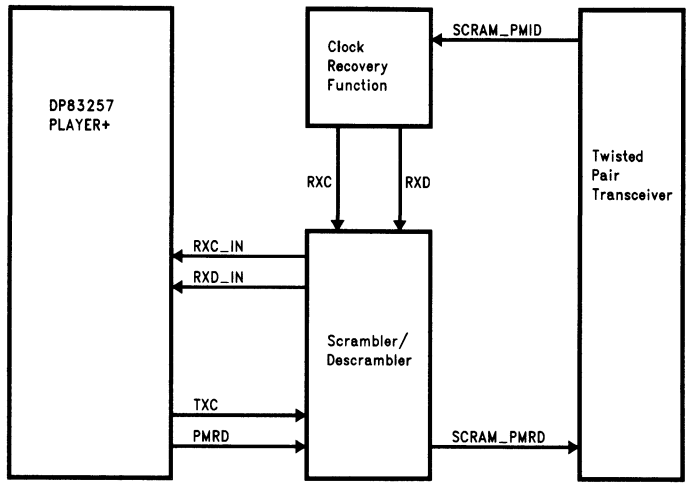

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FIGURE 3-22. PMD Connection with External Clock Recovery

4.0 Modes of Operation

The PLAYER+ device can operate in 4 basic modes: RUN, STOP, LOOPBACK, and CASCADE.

4.1 RUN MODE

RUN is the normal mode of operation.

In this mode, the PLAYER+ device is configured to be connected to the media via the PMD transmitter and PMD receiver at the PMD Interface. It is also connected to any other PLAYER+ device(s) and/or MACSI device(s) via the Port A and Port B Interfaces.

While operating in the RUN mode, the PLAYER+ device receives and transmits Line States (Quiet, Halt, Master, Idle) and frames (Active LIne State).

4.2 STOP MODE

The PLAYER+ device operates in the STOP mode while it is being initialized or configured.

The PLAYER+ device is also reset to the STOP mode automatically when the ~RST pin is set to ground.

When in STOP mode, the PLAYER+ device performs the following functions:

- Resets the Repeat Filter.
- Resets the Smoother.
- Resets the Receiver Block Line State Counters.
- Resets the Clock Recovery Module
- Flushes the Elasticity Buffer.
- Forces Line State Unknown in the Receiver Block.
- Outputs PHY Invalid condition symbol pairs through the PHY Data Indicate pins (AIP, AIC, AID<7:0>, BIP, BIC, BID<7:0>).
- Outputs Quiet symbol pairs through the PMD Data Request pins (PMRD±).
- Resets all Control Bus register contents to zero or default values.

4.3 LOOPBACK MODE

The PLAYER+ device provides 3 types of loopback tests: Configuration Switch Loopback, Short Internal Loopback, and Long Internal Loopback. These Loopback modes can be used to test different portions of the device.

Configuration Switch Loopback

The Configuration Switch Loopback can be used to test the data paths of the MACSI device(s) that are connected to the PLAYER+ device before transmitting and receiving data through the network.

In the Configuration Switch Loopback mode, the PLAYER+ device performs the following functions:

- Selects Port A PHY Request Data, Port B PHY Request Data, or PHY Invalid to connect to Port A PHY Indicate Data via the A__IND Mux.
- Selects Port A PHY Request Data, Port B PHY Request Data, or PHY Invalid to connect to Port B PHY Indicate Data via the B__IND Mux.
- Connects data from the Receiver Block to the Transmitter Block via the Transmitter__Mux. (The PLAYER+ device is repeating incoming data from the media in the Configuration Switch Loopback mode.)

See *Figure 4-1* and *Figure 4-2*.

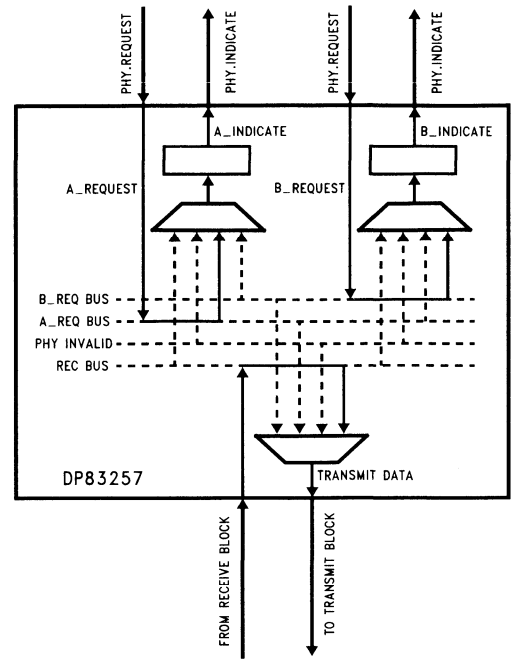

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FIGURE 4-1. Configuration Switch Loopback for DP83257

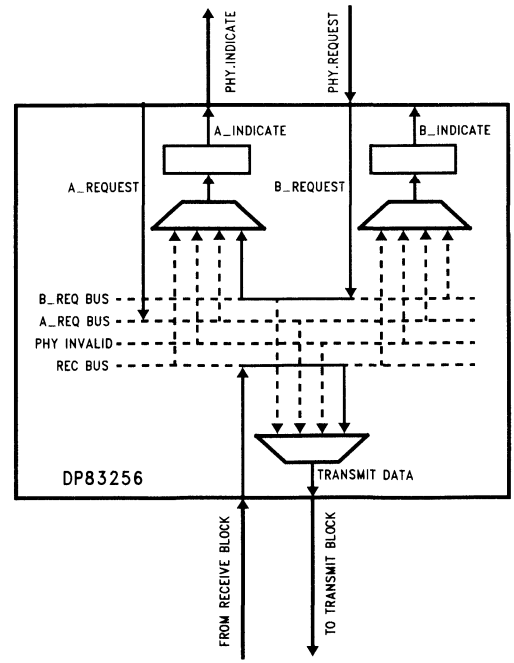

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FIGURE 4-2. Configuration Switch Loopback for DP83256

4.0 Modes of Operation (Continued)

Short Internal Loopback

The Short Internal Loopback mode can be used to test the functionality of the PLAYER+ device, not including the Clock Recovery function, and to test the data paths between the PLAYER+ device and MACSI devices before ring insertion.

When in the Short Internal Loopback mode, the PLAYER+ device performs the following functions:

- Directs the output data of the Transmitter Block to the input of the Receiver Block through an internal path.
- Ignores the PMD Data Indicate pins (PMID±),
- Outputs Quiet symbols through the PMD Data Request pins (PMRD±).

The level of the Quiet symbols transmitted through the PMRD± pins during loopback is automatically set to the transmitter off level.

If both Short Internal Loopback and Long Internal Loopback modes are selected, Long Internal Loopback mode will have priority over Short Internal Loopback mode. This is the longest loopback path within the PLAYER+ device.

See *Figure 4-3*, Short Internal Loopback.

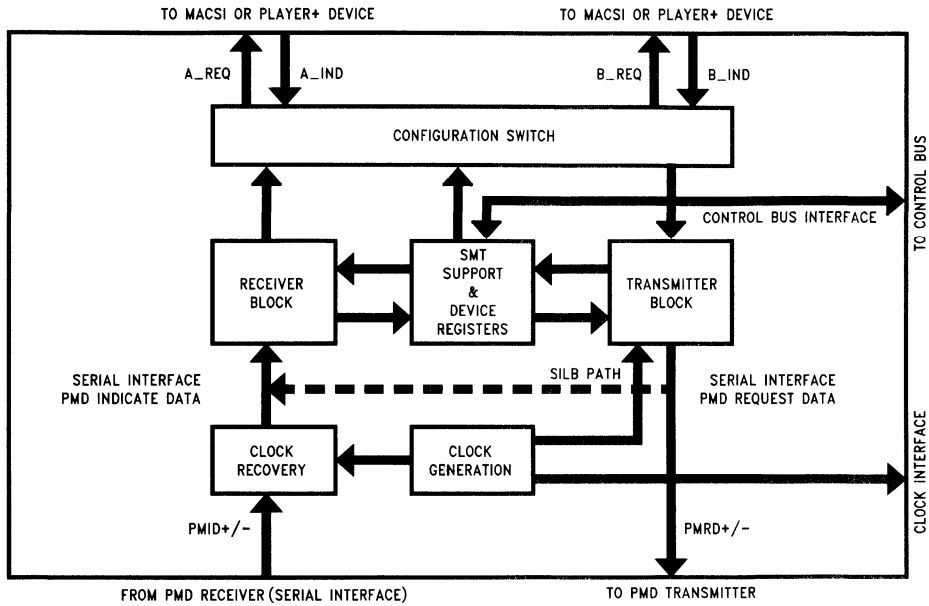

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FIGURE 4-3. Short Internal Loopback

4.0 Modes of Operation (Continued)

Long Internal Loopback

The Long Internal Loopback mode implements the longest loopback path that is completely within the PLAYER+ device.

The Long Internal Loopback mode can be used to test the functionality of the PLAYER+ device, including the Clock Recovery function, and to test the data paths between the PLAYER+ device and MACSI devices before ring insertion.

When in the Long Internal Loopback mode, the PLAYER+ device performs the following functions:

- Directs the output data of the Transmitter Block to the input of the Clock Recovery Module through an internal path.
- Ignores the PMD Data Indicate pins (PMID±),
- Outputs Quiet symbols through the PMD Data Request pins (PMRD±).

The level of the Quiet symbols transmitted through the PMRD± pins during loopback is automatically set to the transmitter off level.

If both Short Internal Loopback and Long Internal Loopback modes are selected, Long Internal Loopback mode will have priority over Short Internal Loopback mode. This is the longest loopback path within the PLAYER+ device.

See *Figure 4-4*, Long Internal Loopback.

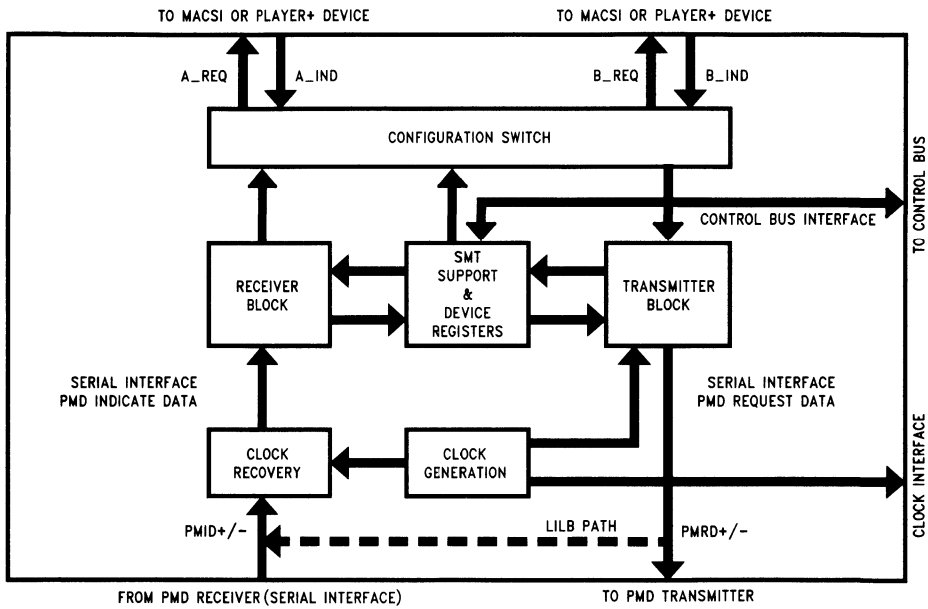

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FIGURE 4-4. Long Internal Loopback

4.0 Modes of Operation (Continued)

4.4 CASCADE MODE

The PLAYER+ device can operate in the Cascade (parallel) mode *(Figure 4-5)* which is used in high bandwidth, point-to-point data transfer applications. This is a non-FDDI mode of operation.

Concepts

In the Cascade mode, multiple PLAYER+ devices are connected together to provide data transfer at multiples of the FDDI data rate. Two cascaded PLAYER+ devices provide a data rate twice the FDDI data rate; three cascaded PLAYER+ devices provide a data rate three times the FDDI data rate, etc.

Multiple data streams are transmitted in parallel over each pair of cascaded PLAYER+ devices. All data streams start simultaneously and begin with the JK symbol pair on each PLAYER+ device.

Data is synchronized at the receiver of each PLAYER+ device by the JK symbol pair. Upon receiving a JK symbol pair, a PLAYER+ device asserts the Cascade Ready signal to indicate the beginning of data reception.

The Cascade Ready signals of all PLAYER+ devices are open drain ANDed together to create the Cascade Start signal. The Cascade Start signal is used as the input to indicate that all PLAYER+ devices have received the JK symbol pair. Data is now being received at every PLAYER+ device and can be transferred from the cascaded PLAYER+ devices to the host system.

See *Figure 4-6* for more information.

Operating Rules

When the PLAYER+ device is operating in Cascade mode, the following rules apply:

1. Data integrity can be guaranteed if the worst case PMD transmission skew between parallel media is less than 40 ns. For example, this amounts to about 785 meters of fiber optic cable, assuming a 1% worst case variance.
2. Even though this is a non-FDDI application, the general rules for FDDI frames must be obeyed.
   - Data frames must be a minimum of three bytes long (including the JK symbol pair). Smaller frames will cause Elasticity Buffer errors.
   - Data frames must have a maximum size of 4500 bytes, with a JK starting delimiter and a T or R or S ending delimiter.
3. Due to the different clock rates, the JK symbol pair may arrive at different times at each PLAYER+ device. The total skew between the fastest and slowest cascaded PLAYER+ devices receiving the JK starting delimiter must not exceed 80 ns.
4. The first PLAYER+ device to receive a JK symbol pair will present it to the host system and release the Cascade Ready signal. The PLAYER+ device will present one more JK as it waits for the other PLAYER+ devices to recognize their JK. The maximum number of consecutive JSs that can be presented to the host is 2.
5. The Cascade Start signal is set to 1 when all the cascaded PLAYER+ devices release their Cascade Ready signals.
6. Bit 4 (CSE) of the Receive Condition Register B (RCRB) is set to 1 if the Cascade Start signal (CS) is **not** set before the second falling edge of clock signal LBC from when Cascade Ready (CR) was released. CS has to be set approximately within 80 ns of CR release. This condition signifies that not all cascaded PLAYER+ devices have received their respective JK symbol pair with the allowed skew range.
7. PLAYER+ devices may not report a Cascaded Synchronization Error if the JK symbols are corrupted in the point-to-point links.
8. To guarantee integrity of the interframe information, the user must put at least 8 Idle symbol pairs between frames. The PLAYER+ device will function properly with only 4 Idle symbol pairs, however the interframe symbols may be corrupted with random non-JK symbols.

The MACSI device could be used to provide the required framing and optional FCS support.

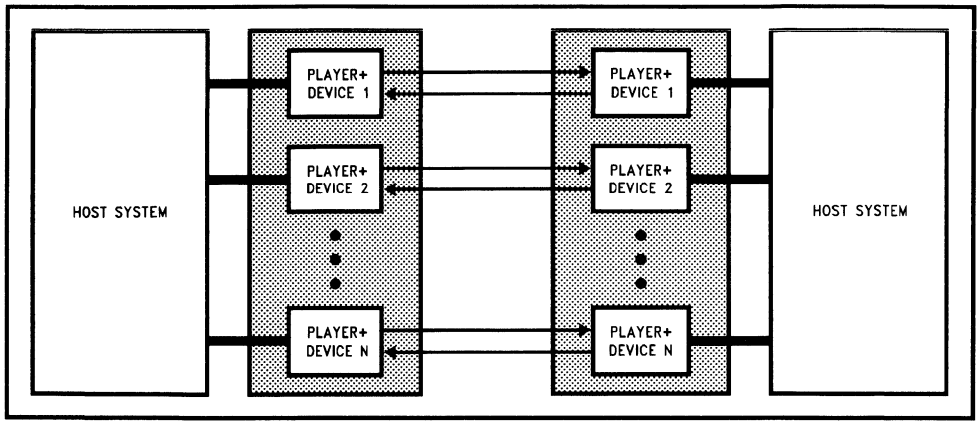

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FIGURE 4-5. Parallel Transmission

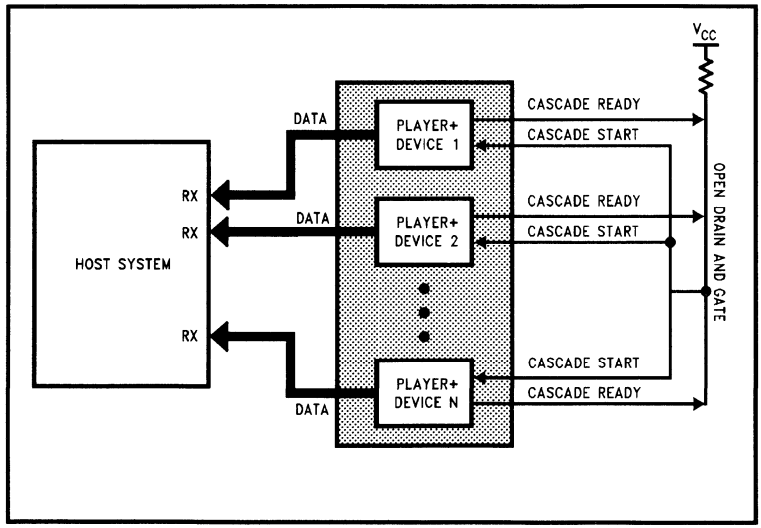

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FIGURE 4-6. Cascade Mode of Operation

5.0 Registers

The PLAYER+ device can be initialized, configured, and monitored using 64 8-bit registers. These registers are accessible through the Control Bus Interface.

The following tables summarize each register's attributes.

Note: RESERVED Registers may be read at any time, although the values read are not specified. The results of RESERVED Register writes are not specified, and may have adverse implications. The user should not write to RESERVED Register locations.

TABLE 5-1. Register Summary

Register Address	Register Symbol	Register Name	Access Rules	
			Read	Write
00h	MR	Mode Register	Always	Always
01h	CR	Configuration Register	Always	Conditional
02h	ICR	Interrupt Condition Register	Always	Conditional
03h	ICMR	Interrupt Condition Mask Register	Always	Always
04h	CTSR	Current Transmit State Register	Always	Conditional
05h	IJTR	Injection Threshold Register	Always	Always
06h	ISRA	Injection Symbol Register A	Always	Always
07h	ISRB	Injection Symbol Register B	Always	Always
08h	CRSR	Current Receive State Register	Always	Write Reject
09h	RCRA	Receive Condition Register A	Always	Conditional
0Ah	RCRB	Receive Condition Register B	Always	Conditional
0Bh	RCMRA	Receive Condition Mask Register A	Always	Always
0Ch	RCMRB	Receive Condition Mask Register B	Always	Always
0Dh	NTR	Noise Threshold Register	Always	Always
0Eh	NPTR	Noise Prescale Threshold Register	Always	Always
0Fh	CNCR	Current Noise Count Register	Always	Write Reject
10h	CNPCR	Current Noise Prescale Count Register	Always	Write Reject
11h	STR	State Threshold Register	Always	Always
12h	SPTR	State Prescale Threshold Register	Always	Always
13h	CSCR	Current State Count Register	Always	Write Reject
14h	CSPCR	Current State Prescale Count Register	Always	Write Reject
15h	LETR	Link Error Threshold Register	Always	Always
16h	CLECR	Current Link Error Count Register	Always	Write Reject
17h	UDR	User Definable Register	Always	Always
18h	IDR	Device ID Register	Always	Write Reject
19h	CIJCR	Current Injection Count Register	Always	Write Reject
1Ah	ICCR	Interrupt Condition Comparison Register	Always	Always
1Bh	CTSCR	Current Transmit State Comparison Register	Always	Always
1Ch	RCCRA	Receive Condition Comparison Register A	Always	Always

TABLE 5-1. Register Summary (Continued)

Register Address	Register Symbol	Register Name	Access Rules	
			Read	Write
1Dh	RCCRB	Receive Condition Comparison Register B	Always	Always
1Eh	MODE2	Mode Register 2	Always	Conditional
1Fh	CMTCCR	CMT Condition Comparison Register	Always	Always
20h	CMTCR	CMT Condition Register	Always	Conditional
21h	CMTMR	CMT Condition Mask Register	Always	Always
22h	RR22	Reserved Register 22	Always	DO NOT WRITE
23h	RR23	Reserved Register 23	Always	DO NOT WRITE
24h	STTR	Scrub Timer Threshold Register	Always	Always
25h	STVR	Scrub Timer Value Register	Always	Write Reject
26h	TDR	Trigger Definition Register	Always	Always
27h	TTCR	Trigger Transition Configuration Register	Always	Always
28h	RR28	Reserved Register 28	Always	DO NOT WRITE
29h	RR29	Reserved Register 29	Always	DO NOT WRITE
2Ah	RR2A	Reserved Register 2A	Always	DO NOT WRITE
2Bh	RR2B	Reserved Register 2B	Always	DO NOT WRITE
2Ch	RR2C	Reserved Register 2C	Always	DO NOT WRITE
2Dh	RR2D	Reserved Register 2D	Always	DO NOT WRITE
2Eh	RR2E	Reserved Register 2E	Always	DO NOT WRITE
2Fh	RR2F	Reserved Register 2F	Always	DO NOT WRITE
30h	RR30	Reserved Register 30	Always	DO NOT WRITE
31h	RR31	Reserved Register 31	Always	DO NOT WRITE
32h	RR32	Reserved Register 32	Always	DO NOT WRITE
33h	RR33	Reserved Register 33	Always	DO NOT WRITE
34h	RR34	Reserved Register 34	Always	DO NOT WRITE
35h	RR35	Reserved Register 35	Always	DO NOT WRITE
36h	RR36	Reserved Register 36	Always	DO NOT WRITE
37h	RR37	Reserved Register 37	Always	DO NOT WRITE
38h	RR38	Reserved Register 38	Always	DO NOT WRITE
39h	RR39	Reserved Register 39	Always	DO NOT WRITE
3Ah	RR3A	Reserved Register 3A	Always	DO NOT WRITE
3Bh	CGMREG	Clock Generation Module Register	Always	Always
3Ch	RR3C	Reserved Register 3C	Always	DO NOT WRITE
3Dh	RR3D	Reserved Register 3D	Always	DO NOT WRITE
3Eh	RR3E	Reserved Register 3E	Always	DO NOT WRITE
3Fh	RR3F	Reserved Register 3F	Always	DO NOT WRITE

5.0 Registers (Continued)

TABLE 5-2. Register Bit Summary

Register Address	Register Symbol	Bit Symbols							
		D7	D6	D5	D4	D3	D2	D1	D0
00h	MR	RNRZ	TNRZ	TE	TQL	CM	EXLB	ILB	RUN
01h	CR	BIE	AIE	TRS1	TRS0	BIS1	BIS0	AIS1	AIS0
02h	ICR	UDI	RCB	RCA	LEMT	CWI	CCR	CPE	DPE
03h	ICMR	UDIM	RCBM	RCAM	LEMTM	CWIM	CCRM	CPEM	DPEM
04h	CTSR	RES	PRDPE	SE	IC1	IC0	TM2	TM1	TM0
05h	IJTR	IJT7	IJT6	IIJ5	IJT4	IJT3	IJT2	IJT1	IJT0
06h	ISRA	RES	RES	RES	IJS4	IJS3	IJS2	IJS1	IJS0
07h	ISRB	RES	RES	RES	IJS9	IJS8	IJS7	IJS6	IJS5
08h	CRSR	RES	RES	RES	RES	LSU	LS2	LS1	LS0
09h	RCRA	LSUPI	LSC	NT	NLS	MLS	HLS	QLS	NSD
0Ah	RCRB	RES	SILS	EBOU	CSE	LSUPV	ALS	ST	ILS
0Bh	RCMRA	LSUPIM	LSCM	NTM	NLSM	MLSM	HLSM	QLSM	NSDM
0Ch	RCMRB	RES	SILSM	EBOUM	CSEM	LSUPVM	ALSM	STM	ILSM
0Dh	NTR	RES	NT6	NT5	NT4	NT3	NT2	NT1	NT0
0Eh	NPTR	NPT7	NPT6	NPT5	NPT4	NPT3	NPT2	NPT1	NPT0
0Fh	CNCR	NCLSCD	CNC6	CNC5	CNC4	CNC3	CNC2	CNC1	CNC0
10h	CNPCR	CNPC7	CNPC6	CNPC5	CNPC4	CNPC3	CNPC2	CNPC1	CNPC0
11h	STR	RES	ST6	ST5	ST4	ST3	ST2	ST1	ST0
12h	SPTR	SPT7	SPT6	SPT5	SPT4	SPT3	SPT2	SPT1	SPT0
13h	CSCR	SCLSCD	CSC6	CSC5	CSC4	CSC3	CSC2	CSC1	CSC0
14h	CSPCR	CSPC7	CSPC6	CSPC5	CSPC4	CSPC3	CSPC2	CSPC1	CSPC0
15h	LETR	LET7	LET6	LET5	LET4	LET3	LET2	LET1	LET0
16h	CLECR	LEC7	LEC6	LEC5	LEC4	LEC3	LEC2	LEC1	LEC0
17h	UDR	RES	RES	RES	RES	EB1	EB0	SB1	SB0
18h	IDR	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
19h	CIJCR	IJC7	IJC6	IJC5	IJC4	IJC3	IJC2	IJC1	IJC0
1Ah	ICCR	UDIC	RCBC	RCAC	LEMTC	CWIC	CCRC	CPEC	DPEC
1Bh	CTSCR	RESC	PRDPEC	SEC	IC1C	IC0C	TM2C	TM1C	TM0C
1Ch	RCCRA	LSUPIC	LSCC	NTC	NLSC	MLSC	HLSC	QLSC	NSDC
1Dh	RCCRB	RESC	SILSC	EBOUC	CSEC	LSUPVC	ALSC	STC	ILSC
1Eh	MODE2	ESTC	RES	CLKSEL	RES	RES	RES	CBPE	PHYRST
1Fh	CMTCCR	TCOC	STEC	RES	RES	RES	RES	RES	RES
20h	CMTCR	TCO	STE	RES	RES	RES	RES	RES	RES
21h	CMTMR	TCOM	STEM	RES	RES	RES	RES	RES	RES
22h	RR22	RES	RES	RES	RES	RES	RES	RES	RES

5.0 Registers (Continued)

TABLE 5-2. Register Bit Summary (Continued)

Register Address	Register Symbol	Bit Symbols							
		D7	D6	D5	D4	D3	D2	D1	D0
23h	RR23	RES	RES	RES	RES	RES	RES	RES	RES
24h	STTR	STT7	STT6	STT5	STT4	STT3	STT2	STT1	STT0
25h	STVR	STV7	STV6	STV5	STV4	STV3	STV2	STV1	STV0
26h	TDR	TONT	TOQLS	TOHLS	TOMLS	TOSILS	TTM2	TTM1	TTM0
27h	TTCR	BIE	AIE	TRS1	TRS0	BIS1	BIS0	AIS1	AIS0
28h	RR28	RES	RES	RES	RES	RES	RES	RES	RES
29h	RR29	RES	RES	RES	RES	RES	RES	RES	RES
2Ah	RR2A	RES	RES	RES	RES	RES	RES	RES	RES
2Bh	RR2B	RES	RES	RES	RES	RES	RES	RES	RES
2Ch	RR2C	RES	RES	RES	RES	RES	RES	RES	RES
2Dh	RR2D	RES	RES	RES	RES	RES	RES	RES	RES
2Eh	RR2E	RES	RES	RES	RES	RES	RES	RES	RES
2Fh	RR2F	RES	RES	RES	RES	RES	RES	RES	RES
30h	RR30	RES	RES	RES	RES	RES	RES	RES	RES
31h	RR31	RES	RES	RES	RES	RES	RES	RES	RES
32h	RR32	RES	RES	RES	RES	RES	RES	RES	RES
33h	RR33	RES	RES	RES	RES	RES	RES	RES	RES
34h	RR34	RES	RES	RES	RES	RES	RES	RES	RES
35h	RR35	RES	RES	RES	RES	RES	RES	RES	RES
36h	RR36	RES	RES	RES	RES	RES	RES	RES	RES
37h	RR37	RES	RES	RES	RES	RES	RES	RES	RES
38h	RR38	RES	RES	RES	RES	RES	RES	RES	RES
39h	RR39	RES	RES	RES	RES	RES	RES	RES	RES
3Ah	RR3A	RES	RES	RES	RES	RES	RES	RES	RES
3Bh	CGMREG	RES	RES	FLTREN	RES	TXCE	RES	RES	RES
3Ch	RR3C	RES	RES	RES	RES	RES	RES	RES	RES
3Dh	RR3D	RES	RES	RES	RES	RES	RES	RES	RES
3Eh	RR3E	RES	RES	RES	RES	RES	RES	RES	RES
3Fh	RR3F	RES	RES	RES	RES	RES	RES	RES	RES

5.0 Registers (Continued)

TABLE 5-3. Register Reset Value Summary

Register Address	Register Symbol	Reset Contents	
		MSB-LSB	Comments
00h	MR	00 h	
01h	CR	00 h	
02h	ICR	X001 0000 B	depends on sense pins
03h	ICMR	00 h	
04h	CTSR	A2 h	
05h	IJTR	00 h	
06h	ISRA	00 h	
07h	ISRB	00 h	
08h	CRSR	0A h	
09h	RCRA	20 h	
0Ah	RCRB	00X0 0010 B	depends on EB state
0Bh	RCMRA	00 h	
0Ch	RCMRB	00 h	
0Dh	NTR	00 h	
0Eh	NPTR	00 h	
0Fh	CNCR	00 h	
10h	CNPCR	00 h	
11h	STR	00 h	
12h	SPTR	00 h	
13h	CSCR	00 h	
14h	CSPCR	00 h	
15h	LETR	00 h	
16h	CLECR	00 h	
17h	UDR	000X 00XX B	depends on sense pins
18h	IDR	XX h	depends on chip version
19h	CIJCR	00 h	
1Ah	ICCR	00 h	same as reg 02 h if reg 02 h is read first
1Bh	CTSCR	00 h	same as reg 04 h if reg 04 h is read first
1Ch	RCCRA	00 h	same as reg 09 h if reg 09 h is read first
1Dh	RCCRB	00 h	same as reg 0A h if reg 0A h is read first

TABLE 5-3. Register Reset Value Summary (Continued)

Register Address	Register Symbol	Reset Contents	
		MSB-LSB	Comments
1Eh	MODE2	00 h	
1Fh	CMTCCR	00 h	
20h	CMTCR	00 h	
21h	CMTMR	00 h	
22h	RR22	XX h	
23h	RR23	XX h	
24h	STTR	00 h	
25h	STVR	00 h	
26h	TDR	00 h	
27h	TTCR	00 h	
28h	RR28	XX h	
29h	RR29	XX h	
2Ah	RR2A	XX h	
2Bh	RR2B	XX h	
2Ch	RR2C	XX h	
2Dh	RR2D	XX h	
2Eh	RR2E	XX h	
2Fh	RR2F	XX h	
30h	RR30	XX h	
31h	RR31	XX h	
32h	RR32	XX h	
33h	RR33	XX h	
34h	RR34	XX h	
35h	RR35	XX h	
36h	RR36	XX h	
37h	RR37	XX h	
38h	RR38	XX h	
39h	RR39	XX h	
3Ah	RR3A	XX h	
3Bh	CGMREG	05 h	
3Ch	RR3C	XX h	
3Dh	RR3D	XX h	
3Eh	RR3E	XX h	
3Fh	RR3F	XX h	

5.0 Registers (Continued)

5.1 MODE REGISTER (MR)

The Mode Register is used to initialize and configure the PLAYER+ device.

ACCESS RULES

ADDRESS	READ	WRITE
00h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
RNRZ	TNRZ	TE	TQL	CM	LILB	SILB	RUN

Bit	Symbol	Description
D0	RUN	**RUN/~STOP:** 0: Enables the STOP mode. Refer to section 4.2, STOP MODE, for more information. 1: Normal operation (i.e. RUN mode). **Note:** The RUN bit is automatically set to 0 when the ~RST pin is asserted (i.e. set to ground).
D1	SILB	**SHORT INTERNAL LOOPBACK:** 0: Disables Internal Loopback mode (i.e. normal operation). 1: Enables Internal Loopback mode. Refer to section 4.3, LOOPBACK MODE, for more information.
D2	LILB	**LONG INTERNAL LOOPBACK:** 0: Disables External Loopback mode (i.e. normal operation). 1: Enables External Loopback mode. Refer to section 4.3, LOOPBACK MODE, for more information.
D3	CM	**CASCADE MODE:** 0: Disables synchronization of cascaded PLAYER+ devices. 1: Enables the synchronization of cascaded PLAYER+ devices. Refer to section 4.4, CASCADE MODE, for more information.
D4	TQL	**TRANSMIT QUIET LEVEL:** This bit is used to program the transmission level of the Quiet symbols during Off Transmit mode (OTM) only. 0: Low (PMD OFF) level Quiet symbols are transmitted through the PMD Data Request pins (i.e. PMRD + = low, PMRD − = high). 1: High (PMD ON) level Quiet symbols are transmitted through the PMD Data Request pins (i.e. PMRD + = high, PMRD − = low).
D5	TE	**TRANSMIT ENABLE:** The TE bit controls the action of the PMD transmitter Enable (TXE) pin. When TE is 0, the TXE output disables the PMD transmitter; when TE is 1, the PMD transmitter is disabled during the Off Transmit Mode (OTM) and enabled otherwise. The On and Off level of the TXE is depended on the PMD transmitter Enable Level (TEL) pin to the PLAYER+ device. The following rules summaries the output of TXE. 1. If TE = 0, then TXE = Off 2. If TE = 1 and OTM, then TXE = Off 3. If TE = 1 and not OTM, then TXE = On.
D6	TNRZ	**TRANSMIT NRZ DATA:** 0: Transmits data in Non-Return-To-Zero-Invert-On-Ones (NRZI) format (normal format). 1: Transmits data in Non-Return-To-Zero format (NRZ).
D7	RNRZ	**RECEIVE NRZ DATA:** 0: Receives data in Non-Return-To-Zero-Invert-On-Ones format (NRZI) (normal format). 1: Receives data in Non-Return-To-Zero format (NRZ).

5.0 Registers (Continued)

5.2 CONFIGURATION REGISTER (CR)

The Configuration Register controls the Configuration Switch Block and enables/disables both the A and B ports.

The CR is conditionally writable because the TTCR can be writing a new value into the register if this feature is enabled.

Note that the A_Request and B_Indicate port are offered only on the DP83257, and not in the DP83256. For further information, refer to section 3.4, CONFIGURATION SWITCH.

ACCESS RULES

ADDRESS	READ	WRITE
01h	Always	Conditional

D7	D6	D5	D4	D3	D2	D1	D0
BIE	AIE	TRS1	TRS0	BIS1	BIS0	AIS1	AIS0

Bit	Symbol	Description
D0, D1	AIS0, AIS1	**A_INDICATE SELECTOR <0, 1>:** The A_Indicate Selector <0, 1> bits selects one of the four Configuration Switch data buses for the A_Indicate output port (AIP, AIC, AID<7:0>). **AIS1 AIS0** 0 0 PHY Invalid Bus 0 1 Receiver Bus 1 0 A_Request Bus 1 1 B_Request Bus
D2, D3	BIS0, BIS1	**B_INDICATE SELECTOR <0, 1>:** The B_Indicate Selector <0, 1> bits selects one of the four Configuration Switch data buses for the B_Indicate output port (BIP, BIC, BID<7:0>) **BIS1 BIS0** 0 0 PHY Invalid Bus 0 1 Receiver Bus 1 0 A_Request Bus 1 1 B_Request Bus **Note:** Even though this bit can be set and/or cleared in the DP83256, it will not affect any I/Os since the DP83256 does not offer a B_Indicate port.
D4, D5	TRS0, TRS1	**TRANSMIT REQUEST SELECTOR <0, 1>:** The Transmit Request Selector <0, 1> bits select one of the four Configuration Switch data buses for the input to the Transmitter Block. **TRS1 TRS0** 0 0 PHY Invalid Bus 0 1 Receiver Bus 1 0 A_Request Bus 1 1 B_Request Bus **Note:** If the PLAYER+ device is in Active Transmit Mode (i.e. the Transmit Mode bits (TM<2:0>) of the Current Transmit State Register (CTSR) are set to 000) and the PHY Invalid Bus is selected, then the PLAYER+ device will transmit a maximum of four Halt symbol pairs and then continuous Idle symbols due to the Repeat Filter when in the Repeat state.
D6	AIE	**A_INDICATE ENABLE:** 0: Disables the A_Indicate output port. The A_Indicate port pins will be tri-stated when the port is disabled. 1: Enables the A_Indicate output port (AIP, AIC, AID<7:0>).
D7	BIE	**B_INDICATE ENABLE:** 0: Disables the B_Indicate output port. The B_Indicate port pins will be tri-stated when the port is disabled. 1: Enables the B_Indicate output port (BIP, BIC, BID<7:0>). **Note:** Even though this bit can be set and/or cleared in the DP83256, it will not affect any I/Os since the DP83256 does not offer a B_Indicate port.

5.0 Registers (Continued)

5.3 INTERRUPT CONDITION REGISTER (ICR)

The Interrupt Condition Register records the occurrence of an internal error event, the detection of Line State, an unsuccessful write by the Control Bus Interface, the expiration of an internal counter, or the assertion of one or more of the User Definable Sense pins.

The Interrupt Condition Register will assert the Interrupt pin (~INT) when one or more bits within the register are set to 1 and the corresponding mask bits in the Interrupt Condition Mask Register (ICMR) are also set to 1.

ACCESS RULES

ADDRESS	READ	WRITE
02h	Always	Conditional

D7	D6	D5	D4	D3	D2	D1	D0
UDI	RCB	RCA	LEMT	CWI	CCR	CPE	DPE

Bit	Symbol	Description
D0	DPE	**PHY__REQUEST__DATA PARITY ERROR:** This bit will be set to 1 when: 1. The PHY Request Data Parity Enable bit (PRDPE) of the Current Transmit State Register (CTSR) is set to 1 and 2. The Transmitter Block detects a parity error in the incoming PHY Request Data. The source of the data can be from the PHY Invalid Bus, the Receive Bus, the A__Bus, or the B__Bus of the Configuration Switch. **Note:** Parity is only checked on data that goes into the transmitter block. This means that any data that is just routed through the configuration switch without going into the transmit block is not checked.
D1	CPE	**Control Bus DATA PARITY ERROR:** This bit will be set to 1 when: The Control Bus Interface detects a parity error in the incoming Control Bus Data (CBD<7:0>), CBP during a write cycle.
D2	CCR	**Control Bus WRITE COMMAND REJECT:** This bit will be set to 1 when an attempt to write into one of the following read-only registers is made: Current Receive State Register (Register 08, CRSR) Current Noise Count Register (Register 0F, CNCR) Current Noise Prescale Count Register (Register 10, CNPCR) Current State Count Register (Register 13, CSCR) Current State Prescale Count Register (Register 14, CSPCR) Current Link Error Count Register (Register 16, CLECR) Device ID Register (Register 18, IDR) Current Injection Count Register (Register 19, CIJCR) Scrub Timer Value Register (Register 25, STVR)

5.0 Registers (Continued)

Bit	Symbol	Description
D3	CWI	**CONDITIONAL WRITE INHIBIT:** Set to 1 when bits within mentioned registers do not match bits in the corresponding compare register. This bit ensures that new (i.e. unread) data is not inadvertently cleared while old data is being cleared through the Control Bus Interface. This bit is set to 1 to indicate that a bit in a condition write register was not written because it had changed since the previous write. The following registers are affected: Interrupt Condition Register (Register 02, ICR) Current Transmit State Register (Register 04, CTSR) Receive Condition Register A (Register 09, RCRA) Receive Condition Register B (Register 0A, RCRB) CMT Condition Register (Register 20, CMTCR) The previous registers are affected when they differ from the value of the corresponding bit in the following registers respectively: Interrupt Condition Compare Register (Register 1A, ICCR) Current Transmit State Compare Register (Register 1B, CTSCR) Receive Condition Compare Register A (Register 1C, RCCRA) Receive Condition Compare Register B (Register 1D, RCCRB) CMT Condition Compare Register (Register 1F, CMTCCR) This bit must be cleared by software. Note that this differs from the MACSI, BMAC and BSI device bits of the same name. The Configuration Register (Register 01, CR) can not be written to during scrubbing.
D4	LEMT	**LINK ERROR MONITOR THRESHOLD:** This bit is set to 1 when the internal 8-bit Link Error Monitor Counter reaches zero. It will remain set and is cleared by software. During the reset process (i.e. ~RST = GND), the Link Error Monitor Threshold bit is set to 1 because the Link Error Monitor Counter is initialized to zero.
D5	RCA	**RECEIVE CONDITION A:** This bit is set to 1 when: 1. One or more bits in the Receive Condition Register A (RCRA) is set to 1 and 2. The corresponding mask bits in the Receive Condition Mask Register A (RCMRA) are also set to 1. In order to clear (i.e. set to 0) the Receive Condition A bit, the bits within the Receive Condition Register A that are set to 1 must first be either cleared or masked.
D6	RCB	**RECEIVE CONDITION B:** This bit is set to 1 when: 1. One or more bits in the Receive Condition Register B (RCRB) is set to 1 and 2. The corresponding mask bits in the Receive Condition Mask Register A (RCMRB) are also set to 1. In order to clear (i.e. set to 0) the Receive Condition B bit, the bits within the Receive Condition Register B that are set to 1 must first be either cleared or masked.
D7	UDI	**USER DEFINABLE INTERRUPT:** This bit is set to 1 when one or any combination of the Sense Bits (SB0, SB1, or SB2) in the User Definable Register (UDR) are set to 1. In order to clear (i.e. set to 0) the User Definable Interrupt Bit, all Sense Bits must be set to 0.

5.0 Registers (Continued)

5.4 INTERRUPT CONDITION MASK REGISTER (ICMR)

The Interrupt Condition Mask Register allows the user to dynamically select which events will generate an interrupt.

The Interrupt pin will be asserted (i.e. ~INT = GND) when one or more bits within the Interrupt Condition Register (ICR) are set to 1 and the corresponding mask bits in this register are also set to 1.

This register is cleared (i.e. set to 0) and all interrupts are initially masked during the reset process.

ACCESS RULES

ADDRESS	READ	WRITE
03h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
UDIM	RCBM	RCAM	LEMTM	CWIM	CCRM	CPEM	DPEM

Bit	Symbol	Description
D0	DPEM	**PHY__REQUEST__DATA PARITY ERROR MASK:** The mask bit for the PHY__Request Data Parity Error bit (DPE) of the Interrupt Condition Register (ICR).
D1	CPEM	**Control Bus DATA PARITY ERROR MASK:** The mask bit for the Control Bus Data Parity Error bit (CPE) of the Interrupt Condition Register (ICR).
D2	CCRM	**Control Bus WRITE COMMAND REJECT MASK:** The mask bit for the Control Bus Write Command Reject bit (CCR) of the Interrupt Condition Register (ICR).
D3	CWIM	**CONDITIONAL WRITE INHIBIT MASK:** The mask bit for the Conditional Write Inhibit bit (CWI) of the Interrupt Condition Register (ICR).
D4	LEMTM	**LINK ERROR MONITOR THRESHOLD MASK:** The mask bit for the Link Error Monitor Threshold bit (LEMT) of the Interrupt Condition Register (ICR).
D5	RCAM	**RECEIVE CONDITION A MASK:** The mask bit for the Receive Condition A bit (RCA) of the Interrupt Condition Register (ICR).
D6	RCBM	**RECEIVE CONDITION B MASK:** The mask bit for the Receive Condition B bit (RCB) of the Interrupt Condition Register (ICR).
D7	UDIM	**USER DEFINABLE INTERRUPT MASK:** The mask bit for the User Definable Interrupt bit (UDI) of the Interrupt Condition Register (ICR).

5.5 CURRENT TRANSMIT STATE REGISTER (CTSR)

The Current Transmit State Register can program the Transmitter Block to internally generate and transmit Idle, Master, Halt, Quiet, or user programmable symbol pairs, in addition to the normal transmission of incoming PHY Request data. The Smoother and PHY Request Data Parity are also enabled and disabled through this register.

When the Trigger Definition register (TDR) is used, the CTSR can automatically be set to a preprogrammed line state when a trigger condition occurs. This capability can be used to implement both PC_React and CF_React.

The Transmit Modes have priority over the Repeat Filter and Smoother outputs. The Injection Symbols have priority over the Transmit Modes.

During the reset process (i.e. ~RST = GND) the Transmit Mode is set to Off (TM<2:0> = 010), the Smoother is enabled (i.e. SE is set to 1), and the Reserved bit (b7) is set to 1. All other bits of this register are cleared (i.e. set to 0) during the reset process.

When the TDR register is used to respond to trigger conditions the CTSR will be blocked when the TDR register transmit mode is copied into the CTSR. The Write Reject bit of the ICR will be set if any writes are attempted at this time.

Note: This register has no effect while the device is in Stop Mode.

ACCESS RULES

ADDRESS	READ	WRITE
04h	Always	Conditional

D7	D6	D5	D4	D3	D2	D1	D0
RES	PRDPE	SE	IC1	IC0	TM2	TM1	TM0

Bit	Symbol	Description
D0, D1, D2	TM0, TM1, TM2	**Transmit Mode <0, 1, 2>:** These bits select one of the 6 transmission modes for the PMD Request Data output port (TXD±).

TM2	TM1	TM0	
0	0	0	**Active Transmit Mode (ATM):** Normal transmission of incoming PHY Request data.
0	0	1	**Idle Transmit Mode (ITM):** Transmission of Idle symbol pairs (11111 11111).
0	1	0	**Off Transmit Mode (OTM):** Transmission of Quiet symbol pairs (00000 00000) and deassertion of the PMD transmitter Enable pin (TXE). **Note:** This is the default transmit mode after reset.
0	1	1	**Reserved:** Reserved for future use. Users are discouraged from using this transmit mode. If selected, however, the transmitter will generate Quiet symbol pairs (00000 00000).
1	0	0	**Master Transmit Mode (MTM):** Transmission of Halt and Quiet symbol pairs (00100 00000).
1	0	1	**Halt Transmit Mode (HTM):** Transmission of Halt symbol pairs (00100 00100).
1	1	0	**Quiet Transmit Mode (QTM):** Transmission of Quiet symbol pairs (00000 00000).
1	1	1	**Reserved:** Reserved for future use. Users are discouraged from using this transmit mode. If selected, however, the transmitter will generate Quiet symbol pairs (00000 00000).

5.0 Registers (Continued)

Bit	Symbol	Description
D3, D4	IC0, IC1	**Injection Control <0, 1>:** These bits select one of the 4 injection modes. The injection modes have priority over data from the Smoother, Repeat Filter, Encoder, and Transmit Modes. IC0 is the only bit of the register that is automatically cleared by the PLAYER+ device after the One Shot Injection is executed. The automatic clear of IC0 during the One Shot mode can be interpreted as a acknowledgment that the One Shot has been completed. **IC1 IC0** 0 0 **No Injection:** The normal transmission of incoming PHY Request data (i.e. symbols are not injected). 0 1 **One Shot:** In one shot mode, the contents of Injection Symbol Register A (ISRA) and Injection Symbol Register B (ISRB) are injected n symbol pairs after a JK, where n is the programmed value of the Injection Count Register (IJCR). If IJCR is set to 0, the JK symbol pair is replaced by ISRA and ISRB. Once the One Shot is executed, the PLAYER+ device automatically sets IC0 to 0, thereby returning to normal transmission of data. 1 0 **Periodic:** In Periodic mode, the contents of Injection Symbol Register A (ISRA) and Injection Symbol Register B (ISRB) are injected every n-th symbol pair, where n is the programmed value of the Injection Count Register (IJCR). If IJCR is set to 0, all data symbols are replaced with ISRA and ISRB. **Note:** The inserted symbol is not automatically aligned to a JK boundary. 1 1 **Continuous:** In Continuous mode, all data symbols are replaced with the contents of Injection Symbol Register A (ISRA) and Injection Symbol Register B (ISRB).
D5	SE	**SMOOTHER ENABLE:** 0: Disables the Smoother. 1: Enables the Smoother. When enabled, the Smoother can redistribute Idle symbol pairs which were added or deleted by the local or upstream receivers. **Note:** Once the counter has started, it will continue to count irrespective of the incoming symbols with the exception of a JK symbol pair.
D6	PRDPE	**PHY_REQUEST DATA PARITY ENABLE:** 0: Disables PHY_Request Data parity. 1: Enables PHY_Request Data parity.
D7	RES	**RESERVED:** Reserved for future use. **Note:** Users are discouraged from using this bit. The reserved bit is set to 1 during the reset process. It may be set or cleared without any effects to the functionality of the PLAYER+ device.

5.0 Registers (Continued)

5.6 INJECTION THRESHOLD REGISTER (IJTR)

The Injection Threshold Register, in conjunction with the Injection Control bits (IC<1:0>) in the Current Transmit State Register (CTSR), set the frequency at which the contents of the Injection Symbol Register A (ISRA) and Injection Symbol Register B (ISRB) are inserted into the data stream. It contains the start value for the Injection Counter.

The Injection Threshold Register value is loaded into the Injection Counter when the counter reaches zero or during every Control Bus Interface write-cycle of this register.

The Injection Counter is an 8-bit down-counter which decrements every 80 ns. It's current value is read for CIJCR.

The counter is active only during One Shot or Periodic Injection Modes (i.e. Injection Control<1:0> bits (IC<1:0>) of the Current Transmit State Register (CTSR) are set to either 01 or 10). The Transmitter Block will replace a data symbol pair with ISRA and ISRB when the counter reaches 0 and the Injection Mode is either One Shot or Periodic.

If the Injection Threshold Register is set to 0 during the One Shot mode, the JK will be replaced with ISRA and ISRB. If the Injection Threshold Register is set to 0 during the Periodic mode, all data symbols are replaced with ISRA and ISRB.

The counter is initialized to 0 during the reset process (i.e. ~RST = GND).

For further information, see the INJECTION CONTROL LOGIC section.

ACCESS RULES

ADDRESS	READ	WRITE
05h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
IJT7	IJT6	IJT5	IJT4	IJT3	IJT2	IJT1	IJT0

Bit	Symbol	Description
D0-D7	IJT0–IJT7	**INJECTION THRESHOLD BIT<0-7>:** Start value for the Injection Counter. IJT0 is the Least Significant Bit (LSB).

5.0 Registers (Continued)

5.7 INJECTION SYMBOL REGISTER A (ISRA)

The Injection Symbol Register A, along with Injection Symbol Register B, contains the programmable value (already in 5B code) that can be inserted to replace the data symbol pairs.

In One Shot mode, ISRA and ISRB are injected n bytes after a JK, where n is the programmed value of the Injection Threshold Register. In the Periodic mode, ISRA and ISRB are injected every n-th symbol pair. In the Continuous mode, all data symbols are replaced with ISRA and ISRB.

ACCESS RULES

ADDRESS	READ	WRITE
06h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
RES	RES	RES	IJS4	IJS3	IJS2	IJS1	IJS0

Bit	Symbol	Description
D0–D4	IJS0–IJS4	**INJECTION SYMBOL BIT<0-4>:** Symbol to be injected. IJS0 is the Least Significant Bit (LSB) and goes out onto the media last.
D5–D7	RES	**RESERVED:** Reserved for future use. **Note:** Users are discouraged from using these bits. The reserved bits are set to 0 during the reset process. They may be set or cleared without any effects to the functionality of the PLAYER+ device.

5.0 Registers (Continued)

5.8 INJECTION SYMBOL REGISTER B (ISRB)

The Injection Symbol Register B, along with Injection Symbol Register A, contains the programmable value (already in 5B code) that will replace the data symbol pairs.

In One Shot mode, ISRA and ISRB are injected n bytes after a JK, where n is the programmed value of the Injection Threshold Register. In the Periodic mode, ISRA and ISRB are injected every n-th symbol pair. In the Continuous mode, all data symbols are replaced with ISRA and ISRB.

ACCESS RULES

ADDRESS	READ	WRITE
07h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
RES	RES	RES	IJS9	IJS8	IJS7	IJS6	IJS5

Bit	Symbol	Description
D0–D4	IJS0–IJS4	**INJECTION SYMBOL BIT <0-4>:** Symbol to be injected. IJS0 is the Least Significant Bit (LSB) and goes out onto the media last.
D5–D7	RES	**RESERVED:** Reserved for future use. **Note:** Users are discouraged from using these bits. The reserved bits are set to 0 during the reset process. They may be set or cleared without any effects to the functionality of the PLAYER+ device.

5.0 Registers (Continued)

5.9 CURRENT RECEIVE STATE REGISTER (CRSR)

The Current Receive State Register represents the current line state being detected by the Receiver Block. When the Receiver Block recognizes a new Line State, the bits corresponding to the previous line state are cleared, and the bits corresponding to the new line state are set.

During the reset process (~RST = GND), the Receiver Block is forced to Line State Unknown (i.e. the Line State Unknown bit (LSU) is set to 1).

Note: Users are discouraged from writing to this register. An attempt to write into this register will cause the PLAYER+ device to ignore the Control Bus write cycle and set the Control Bus Write Command Reject bit (CCR) of the Interrupt Condition Register (ICR) to 1.

ACCESS RULES

ADDRESS	READ	WRITE
08h	Always	Write Reject

D7	D6	D5	D4	D3	D2	D1	D0
RES	RES	RES	RES	LSU	LS2	LS1	LS0

Bit	Symbol	Description
D0, D1, D2	LS0, LS1, LS2	**LINE STATE<0, 1, 2>:** These bits represent the current Line State being detected by the Receiver Block. Once the Receiver Block recognizes a new line state, the bits corresponding to the previous line state are cleared, and the bits corresponding to the new line state are set. **LS2 LS1 LS0** 0 0 0 **Active Line State (ALS):** Received a JK symbol pair (11000 10001), possibly followed by data symbols. 0 0 1 **Idle Line State (ILS):** Received a minimum of two consecutive Idle symbol pairs (11111 11111). 0 1 0 **No Signal Detect (NSD):** The Signal Detect (SD) has been deasserted, indicating that the PLAYER+ device is not receiving data from the PMD receiver or that clock detect is not being received from the Clock Recovery Module. SD is ignored during internal loopback. **Note:** NSD is the default value when the device is in Stop mode. 0 1 1 **Reserved:** Reserved for future use. 1 0 0 **Master Line State (MLS):** Received a minimum of 8 consecutive Halt-Quiet symbol pairs (00100 00000). 1 0 1 **Halt Line State (HLS):** Received a minimum of 8 consecutive Halt symbol pairs (00100 00100). 1 1 0 **Quiet Line State (QLS):** Received a minimum of 8 consecutive Quiet symbol pairs (00000 00000). 1 1 1 **Noise Line State (NLS):** Detected a minimum of 16 noise events. Refer to the Receiver Block description for further information on noise events.
D3	LSU	**LINE STATE UNKNOWN:** The Receiver Block has not detected the minimum conditions to enter a known line state. When the Line State Unknown bit is set, LS<2:0> represent the most recently known line state.
D4-D7	RES	**RESERVED:** Reserved for future use. **Note:** Users are discouraged from using these bits. The reserved bits are reset to 0 during the reset process. They may be set or cleared without any effects to the functionality of the PLAYER+ device.

5.0 Registers (Continued)

5.10 RECEIVE CONDITION REGISTER A (RCRA)

The Receive Condition Register A maintains a historical record of the Line States recognized by the Receiver Block.

When a new Line State is entered, the bit corresponding to that line state is set to 1. The bits corresponding to the previous Line States are not cleared by the PLAYER+ device, thereby maintaining a record of the Line States detected.

The Receive Condition A bit (RCA) of the Interrupt Condition Register (ICR) will be set to 1 when one or more bits within the Receive Condition Register A is set to 1 and the corresponding mask bit(s) in Receive Condition Mask Register A (RCMRA) is also set to 1.

ACCESS RULES

ADDRESS	READ	WRITE
09h	Always	Conditional

D7	D6	D5	D4	D3	D2	D1	D0
LSUPI	LSC	NT	NLS	MLS	HLS	QLS	NSD

Bit	Symbol	Description
D0	NSD	**NO SIGNAL DETECT:** Indicates that the Signal Detect pin (TTLSD) has been deasserted and that the Clock Recovery Module is not receiving data from the PMD receiver.
D1	QLS	**QUIET LINE STATE:** Received a minimum of eight consecutive Quiet symbol pairs (00000 00000).
D2	HLS	**HALT LINE STATE:** Received a minimum of eight consecutive Halt symbol pairs (00100 00100).
D3	MLS	**MASTER LINE STATE:** Received a minimum of eight consecutive Halt-Quiet symbol pairs (00100 00000).
D4	NLS	**NOISE LINE STATE:** Detected a minimum of sixteen noise events.
D5	NT	**NOISE THRESHOLD:** This bit is set to 1 when the internal Noise Counter reaches 0. It will remain set until a value equal to or greater than one is loaded into the Noise Threshold Register or Noise Prescale Threshold Register. During the reset process (i.e. ~RST = GND), since the Noise Counter is initialized to 0, the Noise Threshold bit will be set to 1.
D6	LSC	**LINE STATE CHANGE:** A line state change has been detected.
D7	LSUPI	**LINE STATE UNKNOWN AND PHY INVALID:** The Receiver Block has not detected the minimum conditions to enter a known line state. In addition, the most recently known line state was one of the following line states: No Signal Detect, Quiet Line State, Halt Line State, Master Line State, or Noise Line State.

5.0 Registers (Continued)

5.11 RECEIVE CONDITION REGISTER B (RCRB)

The Receive Condition Register B maintains a historical record of the Lines States recognized by the Receiver Block.

When a new Line State is entered, the bit corresponding to that line state is set to 1. The bits corresponding to the previous Line States are not cleared, thereby maintaining a record of the Line States detected.

The Receive Condition B bit (RCB) of the Interrupt Condition Register (ICR) will be set to 1 when one or more bits within the Receive Condition Register B is set to 1 and the corresponding mask bit(s) in Receive Condition Mask Register B (RCMRB) is also set to 1.

ACCESS RULES

ADDRESS	READ	WRITE
0Ah	Always	Conditional

D7	D6	D5	D4	D3	D2	D1	D0
RES	SILS	EBOU	CSE	LSUPV	ALS	ST	ILS

Bit	Symbol	Description
D0	ILS	**IDLE LINE STATE:** Received a minimum of two consecutive Idle symbol pairs (11111 11111).
D1	ST	**STATE THRESHOLD:** This bit will be set to 1 when the internal State Counter reaches zero. It will remain set until a value equal to or greater than one is loaded into the State Threshold Register or State Prescale Threshold Register, and this register is cleared. During the reset process (i.e. ~RST = GND), since the State Counter is initialized to 0, the State Threshold bit is set to 1.
D2	ALS	**ACTIVE LINE STATE:** Received a JK symbol pair (11000 10001), and possibly data symbols following.
D3	LSUPV	**LINE STATE UNKNOWN AND PHY VALID:** The Receiver Block has not detected the minimum conditions to enter a known line state. In addition, the most recently known line state was either Active Line State or Idle Line State.
D4	CSE	**CONNECTION SERVICE EVENT/CASCADE SYNCHRONIZATION ERROR:** When one or more bits in the CMT Condition Register (CMTCR) are set and the corresponding bit(s) in the CMT Condition Mask Register (CMTCMR) are set, the Connection service event bit will be set to a 1. When a synchronization error occurs, the Cascade Synchronization Error bit is set to 1. A synchronization error occurs if the Cascade Start signal (CS) is not asserted within approximately 80 ns of Cascade Ready (CR) release. **Note:** Cascade mode and the CMT features can not be used at the same time.
D5	EBOU	**ELASTICITY BUFFER UNDERFLOW / OVERFLOW:** The Elasticity Buffer has either overflowed or underflowed. The Elasticity Buffer will automatically recover if the condition which caused the error is only transient, but the event bit will remain set until cleared by software.
D6	SILS	**SUPER IDLE LINE STATE:** Received a minimum of eight Idle symbol pairs (11111 11111).
D7	RES	**RESERVED:** Reserved for future use. **Note:** Users are discouraged from using these bits. The reserved bits are reset to 0 during the reset process. They may be set or cleared without any effects to the functionality of the PLAYER+ device

5.0 Registers (Continued)

5.12 RECEIVE CONDITION MASK REGISTER A (RCMRA)

The Receive Condition Mask Register A allows the user to dynamically select which events will generate an interrupt.

The Receive Condition A bit (RCA) of the Interrupt Condition Register (ICR) will be set to 1 when one or more bits within the Receive Condition Register A (RCRA) is set to 1 and the corresponding mask bit(s) in this register is also set to 1.

Since this register is cleared (i.e. set to 0) during the reset process, all interrupts are initially masked.

ACCESS RULES

ADDRESS	READ	WRITE
0Bh	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
LSUPIM	LSCM	NTM	NLSM	MLSM	HLSM	QLSM	NSDM

Bit	Symbol	Description
D0	NSDM	**NO SIGNAL DETECT MASK:** The mask bit for the No Signal Detect bit (NSD) of the Receive Condition Register A (RCRA).
D1	QLSM	**QUIET LINE STATE MASK:** The mask bit for the Quiet Line State bit (QLS) of the Receive Condition Register A (RCRA).
D2	HLSM	**HALT LINE STATE MASK:** The mask bit for the Halt Line State bit (HLS) of the Receive Condition Register A (RCRA).
D3	MLSM	**MASTER LINE STATE MASK:** The mask bit for the Master Line State bit (MLS) of the Receive Condition Register A (RCRA).
D4	NLSM	**NOISE LINE STATE MASK:** The mask bit for the Noise Line State bit (NLS) of the Receive Condition Register A (RCRA).
D5	NTM	**NOISE THRESHOLD MASK:** The mask bit for the Noise Threshold bit (NT) of the Receive Condition Register A (RCRA).
D6	LSCM	**LINE STATE CHANGE MASK:** The mask bit for the Line State Change bit (LSC) of the Receive Condition Register A (RCRA).
D7	LSUPIM	**LINE STATE UNKNOWN AND PHY INVALID MASK:** The mask bit for the Line State Unknown and PHY Invalid bit (LSUPI) of the Receive Condition Register A (RCRA).

5.0 Registers (Continued)

5.13 RECEIVE CONDITION MASK REGISTER B (RCMRB)

The Receive Condition Mask Register B allows the user to dynamically select which events will generate an interrupt.

The Receive Condition B bit (RCB) of the Interrupt Condition Register (ICR) will be set to 1 when one or more bits within the Receive Condition Register B (RCRA) is set to 1 and the corresponding mask bits in this register is also set to 1.

Since this register is cleared (i.e. set to 0) during the reset process, all interrupts are initially masked.

ACCESS RULES

ADDRESS	READ	WRITE
0Ch	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
RESM	SILSM	EBOUM	CSEM	LSUPVM	ALSM	STM	ILSM

Bit	Symbol	Description
D0	ILSM	**IDLE LINE STATE MASK:** The mask bit for the Idle Line State bit (ILS) of the Receive Condition Register B (RCRB).
D1	STM	**STATE THRESHOLD MASK:** The mask bit for the State Threshold bit (ST) of the Receive Condition Register B (RCRB).
D2	ALSM	**ACTIVE LINE STATE MASK:** The mask bit for the Active Line State bit (ALS) of the Receive Condition Register B (RCRB).
D3	LSUPVM	**LINE STATE UNKNOWN AND PHY VALID MASK:** The mask bit for the Line State Unknown and PHY Valid bit (LSUPV) of the Receive Condition Register B (RCRB).
D4	CSEM	**CASCADE SYNCHRONIZATION ERROR MASK/CONNECTION SERVICE EVENT MASK:** The mask bit for the Cascade Synchronization Error/Connection service event bit (CSE) of the Receive Condition Register B (RCRB).
D5	EBOUM	**ELASTICITY BUFFER OVERFLOW/UNDERFLOW MASK:** The mask bit for the Elasticity Buffer Overflow/ Underflow bit (EBOU) of the Receive Condition Register B (RCRB).
D6	SILSM	**SUPER IDLE LINE STATE MASK:** The mask bit for the Super Idle Line State bit (SILS) of the Receive Condition Register B (RCRB).
D7	RESM	**RESERVED MASK:** The mask bit for the Reserved bit (RES) of the Receive Condition Register B (RCRB).

5.0 Registers (Continued)

5.14 NOISE THRESHOLD REGISTER (NTR)

The Noise Threshold Register contains the start value for the Noise Timer. This threshold register is used in conjunction with the Noise Prescale Threshold register for setting the maximum allowable time between entry to ILS, HLS, MLS, ALS, or NSD line states. The Noise timer is used to implement the TNE timing requirement of PCM. The Noise timer decrements by one for every 80 x (NPTR + 1) ns in case of Noise events. As a result, the internal noise counter takes the following amount of time to reach zero:

$$((NPTR + 1) \times NTR + NPTR) \times 80 \text{ ns}$$

The threshold values for the Noise Counter and Noise Prescale Counter are simultaneously loaded into both counters if one of the following conditions is true:

1. Both the Noise Counter and Noise Prescale Counter reach zero and the current Line State is either Noise Line State, Active Line State, or Line State Unknown.

or

2. The current Line State is either Halt Line State, Idle Line State, Master Line State, Quiet Line State, or No Signal Detect.

or

3. The Noise Threshold Register or Noise Prescale Threshold Register goes through a Control Bus Interface write cycle.

In addition, the value of the Noise Prescale Threshold register is loaded into the Noise Prescale Counter if the Noise Prescale Counter reaches zero.

The Noise Counter and Noise Prescale Counter will continue to count, without resetting or reloading the threshold values, if a Line State change occurs and the new line state is either Noise Line State, Active Line State, or Line State Unknown.

When both the Noise Threshold Counter and Noise Counter both reach zero, the Noise Threshold bit of the Receive Condition Register A will be set.

The recommended default value for the NTR register is 40h and for the NPTR register is F9h which corresponds to 1.3 ms as specified in the ANSI standard.

ACCESS RULES

ADDRESS	READ	WRITE
0Dh	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
RES	NT6	NT5	NT4	NT3	NT2	NT1	NT0

Bit	Symbol	Description
D0-D6	NT0-NT6	**NOISE THRESHOLD BIT<0-6>:** Start value for the Noise Counter. NT0 is the Least Significant Bit (LSB).
D7	RES	**RESERVED:** Reserved for future use. **Note:** Users are discouraged from using this bit. Write data is ignored since the reserved bit is permanently set to 0.

5.0 Registers (Continued)

5.15 NOISE PRESCALE THRESHOLD REGISTER (NPTR)

The Noise Prescale Threshold Register contains the start value for the Noise Prescale Timer. This threshold register is used in conjunction with the Noise Threshold register for setting the maximum allowable time between entry to ILS, HLS, MLS, ALS, or NSD. The Noise timer is used to implement the TNE timing requirement of PCM. The Noise Prescale threshold controls how often the Noise timer is decremented. When the Noise Prescale Timer reaches zero, it reloads the count with the contents of the Noise Prescale Threshold Register and also causes the Noise Timer to decrement.

The threshold values for the Noise Counter and Noise Prescale Counter are simultaneously loaded into both counters if one of the following conditions is true:

1. Both the Noise Counter and Noise Prescale Counter reach zero and the current Line State is either Noise Line State, Active Line State, or Line State Unknown.

or

2. The Current Line State is either Halt Line State. Idle Line State, Master Line State, Quiet Line State, or No Signal Detect

or

3. The Noise Threshold Register or Noise Prescale Threshold Register goes through a Control Bus Interface write cycle.

In addition, the value of the Noise Prescale Threshold Register is loaded into the Noise Prescale Counter if the Noise Prescale Counter reaches zero.

The Noise Counter and Noise Prescale Counter will continue to count, without resetting or reloading the threshold values, if a Line State change occurs and the new line state is either Noise Line State, Active Line State, or Line State Unknown.

When both the Noise Threshold Counter and Noise Counter both reach zero, the Noise Threshold bit of the Receive Condition Register A will be set.

See the NTR register description for default value recommendations.

ACCESS RULES

ADDRESS	READ	WRITE
0Eh	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
NPT7	NPT6	NPT5	NPT4	NPT3	NPT2	NPT1	NPT0

Bit	Symbol	Description
D0-D7	NPT0-NPT7	**NOISE PRESCALE THRESHOLD BIT <0-7>:** Start value for the Noise Prescale Timer. NPT0 is the Least Significant Bit (LSB).

5.0 Registers (Continued)

5.16 CURRENT NOISE COUNT REGISTER (CNCR)

The Current Noise Count Register takes a snap-shot of the Noise Timer during every Control Bus Interface read cycle of this register.

During a Control Bus Interface write cycle, the Control Bus Write Command Reject bit (CCR) of the Interrupt Condition Register (ICR) will be set to 1 and will ignore a write cycle.

ACCESS RULES

ADDRESS	READ	WRITE
0Fh	Always	Write Reject

D7	D6	D5	D4	D3	D2	D1	D0
NCLSCD	CNC6	CNC5	CNC4	CNC3	CNC2	CNC1	CNC0

Bit	Symbol	Description
D0–D6	CNC0–CNC6	**CURRENT NOISE COUNT BIT <0-6>:** Snapshot of the Noise Counter.
D7	NCLSCD	**NOISE COUNTER LINE STATE CHANGE DETECTION**

5.0 Registers (Continued)

5.17 CURRENT NOISE PRESCALE COUNT REGISTER (CNPCR)

The Current Noise Prescale Count Register takes a snap-shot of the Noise Prescale Timer during every Control Bus Interface read cycle of this register.

During a Control Bus Interface write cycle, the Control Bus Write Command Reject bit (CCR) of the Interrupt Condition Register (ICR) will be set to 1 and will ignore a write cycle.

ACCESS RULES

ADDRESS	READ	WRITE
10h	Always	Write Reject

D7	D6	D5	D4	D3	D2	D1	D0
CNPC7	CNPC6	CNPC5	CNPC4	CNPC3	CNPC2	CNPC1	CNPC0

Bit	Symbol	Description
D0–D7	CNPC0–7	**CURRENT NOISE PRESCALE COUNT BIT <0–7>:** Snapshot of the Noise Prescale Timer.

5.0 Registers (Continued)

5.18 STATE THRESHOLD REGISTER (STR)

The State Threshold Register contains the start value for the State Timer. This timer is used in conjunction with the State Prescale Timer to count the Line State duration. The State Timer will decrement every 80 ns if the State Prescale Timer is zero and the current Line State is Halt Line State, Idle Line State, Master Line State, Quiet Line State, or No Signal Detect. The State Timer takes

$$((SPTR + 1) \times STR + SPTR) \times 80 \text{ ns}$$

to reach zero during a continuous line state condition.

The threshold values for the State Timer and State Prescale Timer are simultaneously loaded into both counters if one of the following conditions is true:

1. Both the State Timer and State Prescale Timer reach zero and the current Line State is Halt Line State, Idle Line State, Master Line State, Quiet Line State, or No Signal Detect.

or

2. A line state change occurs and the new Line State is Halt Line State, Idle Line State, Master Line State, Quiet Line State, or No Signal Detect.

or

3. The State Threshold Register or State Prescale Threshold Register goes through a Control Bus Interface write cycle.

In addition, the value of the State Prescale Threshold Register is loaded into the State Prescale Counter if the State Prescale Timer reaches zero.

The State Timer and State Prescale Timer will reset by reloading the threshold values, if a Line State change occurs and the new Line State is Halt Line State, Idle Line State, Master Line State, Quiet Line State, or No Signal Detect. On detection of ALS, NLS, or LSU the timer will not decrement.

ACCESS RULES

ADDRESS	READ	WRITE
11h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
RES	ST6	ST5	ST4	ST3	ST2	ST1	ST0

Bit	Symbol	Description
D0-D6	ST0-ST6	**STATE THRESHOLD BIT<0-6>:** Start value for the State Timer. ST0 is the Least Significant Bit (LSB).
D7	RES	**RESERVED:** Reserved for future use. **Note:** Users are discouraged from using this bit. Write data is ignored since the reserved bit is permanently set to 0.

5.0 Registers (Continued)

5.19 STATE PRESCALE THRESHOLD REGISTER (SPTR)

The State Prescale Threshold Register contains the start value for the State Prescale Timer. The State Prescale Timer is a down counter. It is used in conjunction with the State Timer to count the Line State duration.

The threshold values for the State Timer and State Prescale Timer are simultaneously loaded into both timers if one of the following conditions is true:

1. Both the State Timer and State Prescale Timer reach zero and the current Line State is Halt Line State, Idle Line State, Master Line State, Quiet Line State, or No Signal Detect.

or

2. A Line State change occurs and the new Line State is Halt Line State, Idle Line State, Master Line State, Quiet Line State, or No Signal Detect.

or

3. The State Threshold Register or State Prescale Threshold Register goes through a Control Bus Interface write cycle.

The State Prescale Timer will decrement every 80 ns if the current Line State is Halt Line State, Idle Line State, Master Line State, Quiet Line State, or No Signal Detect.

ACCESS RULES

ADDRESS	READ	WRITE
12h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
SPT7	SPT6	SPT5	SPT4	SPT3	SPT2	SPT1	SPT0

Bit	Symbol	Description
D0–D7	SPT0–SPT7	**STATE PRESCALE THRESHOLD BIT <0–7>:** Start value for the State Prescale Timer. SPT0 is the Least Significant Bit (LSB).

5.0 Registers (Continued)

5.20 CURRENT STATE COUNT REGISTER (CSCR)

The Current State Count Register takes a snap-shot of the State Counter during every Control Bus Interface read cycle of this register.

During a Control Bus Interface write cycle, the Control Bus Write Command Reject bit (CCR) of the Interrupt Condition Register (ICR) will be set to 1 and will ignore a write cycle.

ACCESS RULES

ADDRESS	READ	WRITE
13h	Always	Write Reject

D7	D6	D5	D4	D3	D2	D1	D0
SCLSCD	CSC6	CSC5	CSC4	CSC3	CSC2	CSC1	CSC0

Bit	Symbol	Description
D0–D6	CSC0–CSC6	**CURRENT STATE COUNT BIT <0–6>:** Snapshot of the State Counter.
D7	SCLSCD	**STATE COUNTER LINE STATE CHANGE DETECTION**

5.0 Registers (Continued)

5.21 CURRENT STATE PRESCALE COUNT REGISTER (CSPCR)

The Current State Prescale Count Register takes a snap-shot of the State Prescale Counter during every Control Bus Interface read cycle of this register.

During a Control Bus Interface write cycle, the Control Bus Write Command Reject bit (CCR) of the Interrupt Condition Register (ICR) will be set to 1 and will ignore a write cycle.

ACCESS RULES

ADDRESS	READ	WRITE
14h	Always	Write Reject

D7	D6	D5	D4	D3	D2	D1	D0
CSPC7	CSPC6	CSPC5	CSPC4	CSPC3	CSPC2	CSPC1	CSPC0

Bit	Symbol	Description
D0–D7	CSPC0–7	**CURRENT STATE PRESCALE COUNT <0–7>:** Snapshot of the State Prescale Counter.

5.22 LINK ERROR THRESHOLD REGISTER (LETR)

The Link Error Threshold Register contains the start value for the Link Error Monitor Counter. It is an 8-bit down-counter which decrements if link errors are detected.

When the Counter reaches 0, the Link Error Monitor Threshold Register value is loaded into the Link Error Monitor Counter and the Link Error Monitor Threshold bit (LEMT) of the Interrupt Condition Register (ICR) is set to one.

The Link Error Monitor Threshold Register value is also loaded into the Link Error Monitor Counter during every Control Bus Interface write cycle of LETR.

The counter is initialized to 0 during the reset process (i.e. ~RST = GND).

ACCESS RULES

ADDRESS	READ	WRITE
15h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
LET7	LET6	LET5	LET4	LET3	LET2	LET1	LET0

Bit	Symbol	Description
D0–D7	LET0–LET7	**LINK ERROR THRESHOLD BIT <0–7>:** Start value for the Link Error Monitor Counter. LET0 is the Least Significant Bit (LSB).

5.0 Registers (Continued)

5.23 CURRENT LINK ERROR COUNT REGISTER (CLECR)

The Current Link Error Count Register takes a snap-shot of the Link Error Monitor Counter during every Control Bus Interface read cycle of this register.

During a Control Bus Interface write cycle, the Control Bus Write Command Reject bit (CCR) of the Interrupt Condition Register (ICR) will be set to 1 and will ignore a write cycle.

ACCESS RULES

ADDRESS	READ	WRITE
16h	Always	Write Reject

D7	D6	D5	D4	D3	D2	D1	D0
LEC7	LEC6	LEC5	LEC4	LEC3	LEC2	LEC1	LEC0

Bit	Symbol	Description
D0–D7	LEC0–LEC7	**LINK ERROR COUNT BIT <0–7>:** Snapshot of the Link Error Monitor Counter.

5.0 Registers (Continued)

5.24 USER DEFINABLE REGISTER (UDR)

The User Definable Register is used to monitor and control events which are external to the PLAYER+ device.

The value of the Sense Bits reflect the asserted/deasserted state of their corresponding Sense pins. On the other hand, the Enable bits assert/deassert the Enable pins.

Note: SB2 and EB2 are only effective for the DP83257.

ACCESS RULES

ADDRESS	READ	WRITE
17h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
RES	EB2	RES	SB2	EB1	EB0	SB1	SB0

Bit	Symbol	Description
D0	SB0	**SENSE BIT 0:** This bit is set to 1 if the Sense Pin 0 (SP0) is asserted (i.e. SP0 = V_{CC}) for a minimum of 160 ns. Once the asserted signal is latched, Sense Bit 0 can only be cleared through the Control Bus Interface, even if the signal is deasserted. This ensures that the Control Bus Interface will record the source of events which can cause interrupts in a traceable manner.
D1	SB1	**SENSE BIT 1:** This bit is set to 1 if the Sense Pin 1 (SP1) is asserted (i.e. SP1 = V_{CC}) for a minimum of 160 ns. Once the asserted signal is latched, Sense Bit 1 can only be cleared through the Control Bus Interface, even if the signal is deasserted. This ensures that the Control Bus Interface will record the source of events which can cause interrupts in a traceable manner.
D2	EB0	**ENABLE BIT 0:** The Enable Bit 0 allows control of external logic through the Control Bus Interface. The User Definable Enable Pin 0 (EP0) is asserted/deasserted by this bit. 0: EP0 is deasserted (i.e. EP0 = GND). 1: EP0 is asserted (i.e. EP0 = V_{CC}).
D3	EB1	**ENABLE BIT 1:** This bit allows control of external logic through the Control Bus Interface. The User Definable Enable Pin 0 (EP0) is asserted/deasserted by this bit. 0: EP1 is deasserted (i.e. EP1 = GND). 1: EP1 is asserted (i.e. EP1 = V_{CC}).
D4	SB2	**SENSE BIT 2:** This bit is set to 1 if the Sense Pin 2 (SP2) is asserted (i.e. SP2 = V_{CC}) for a minimum of 160 ns. Once the asserted signal is latched, Sense Bit 2 can only be cleared through the Control Bus Interface, even if the signal is deasserted. This ensures that the Control Bus Interface will record the source of events which can cause interrupts in a traceable manner. **Note:** SB2 and EB2 are only effective for the DP83257.
D5	RES	**RESERVED:** Reserved for future use. The reserved bit is set to 0 during the initialization process (i.e. ~RST = GND). **Note:** Users are discouraged from using this bit. It may be set or cleared without any effects to the functionality of the PLAYER+ device.
D6	EB2	**ENABLE BIT2:** The Enable Bit 2 allows control of external logic through the Control Bus Interface. The User Definable Enable Pin 2 (EP2) is asserted/deasserted by this bit. **Note:** SB2 and EB2 are only effective for the DP83257. 0: EP2 is deasserted (i.e. EP2 = GND). 1: EP2 is asserted (i.e. EP2 = V_{CC}).
D7	RES	**RESERVED:** Reserved for future use. The reserved bit is set to 0 during the initialization process (i.e. ~RST = GND). **Note:** Users are discouraged from using this bit. It may be set or cleared without any effects to the functionality of the PLAYER+ device.

5.0 Registers (Continued)

5.25 DEVICE ID REGISTER (DIR)

The Device ID Register contains the binary equivalent of the revision number for this device. It can be used to ensure proper software and hardware versions are matched.

During a Control Bus Interface write cycle, the Control Bus Write Command Register bit (CCR) of the Interrupt Condition Register (ICR) will be set to 1, and will ignore write cycle.

ACCESS RULES

ADDRESS	READ	WRITE
18h	Always	Write Reject

D7	D6	D5	D4	D3	D2	D1	D0
DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0

Bit	Symbol	Description
D0–D3	DID0–DID3	**DEVICE ID BIT <0-3>:** Circuit enhancement revision number. Bit 3 is the MSB. The initial revision of the PLAYER+ is equal to 0 and enhancements will increment this number.
D4–D7	DID4–DID7	**DEVICE ID BIT <4-7>:** Architecture level of the PHY device. Bit 7 is the MSB. The original PLAYER device was equal to 0 and the PLAYER+ is equal to 1. This number will only be incremented after a significant architectural change.

5.26 CURRENT INJECTION COUNT REGISTER (CIJCR)

The Current Injection Count Register takes a snap-shot of the Injection Counter during every Control Bus Interface read cycle of this register.

During a Control Bus Interface write cycle, the Control Bus Write Command Reject bit (CCR) of the Interrupt Condition Register (ICR) will be set to 1 and will ignore a write cycle.

The Injection Counter is an 8-bit down-counter which decrements every 80 ns.

The counter is active only during One Shot or Periodic Injection Modes (i.e. Injection Control<1:0> bits (IC<1:0>) of the Current Transmit State Register (CTSR) are set to either 01 or 10).

The Injection Threshold Register (IJTR) value is loaded into the Injection Counter when the counter reaches zero and during every Control Bus Interface write cycle of IJTR.

The counter is initialized to 0 during the reset process (i.e. ~RST = GND).

ACCESS RULES

ADDRESS	READ	WRITE
19h	Always	Write Reject

D7	D6	D5	D4	D3	D2	D1	D0
IJC7	IJC6	IJC5	IJC4	IJC3	IJC2	IJC1	IJC0

Bit	Symbol	Description
D0–D7	IJC0–IJC7	**INJECTION COUNT BIT<0-7>:** Current value of the Injection Counter. IJC0 is the Least Significant Bit (LSB).

5.0 Registers (Continued)

5.27 INTERRUPT CONDITION COMPARISON REGISTER (ICCR)

The Interrupt Condition Comparison Register ensures that the Control Bus must first read a bit modified by the PLAYER+ device before it can be written to by the Control Bus Interface.

The current state of the Interrupt Condition Register (ICR) is automatically written into the Interrupt Condition Comparison Register (i.e. ICCR = ICR) during a Control Bus Interface read-cycle of ICR.

During a Control Bus Interface write cycle, the PLAYER+ device will set the Conditional Write Inhibit bit (CWI) of the Interrupt Condition Register (ICR) to 1 and disallow the setting or clearing of a bit within ICR when the value of a bit in ICR differs from the value of the corresponding bit in the interrupt Condition Comparison Register.

ACCESS RULES

ADDRESS	READ	WRITE
1Ah	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
UDIC	RCBC	RCAC	LEMTC	CWIC	CCRC	CPEC	DPEC

Bit	Symbol	Description
D0	DPEC	**PHY_REQUEST DATA PARITY ERROR COMPARISON:** The comparison bit for the PHY_Request Data Parity Error bit (DPE) of the Interrupt Condition Register (ICR).
D1	CPEC	**CONTROL BUS DATA PARITY ERROR COMPARISON:** The comparison bit for the Control Bus Data Parity Error bit (CPE) of the Interrupt Condition Register (ICR).
D2	CCRC	**CONTROL BUS WRITE COMMAND REJECT COMPARISON:** The comparison bit for the Control Bus Write Command Reject bit (CCR) of the Interrupt Condition Register (ICR).
D3	CWIC	**CONDITIONAL WRITE INHIBIT COMPARISON:** The comparison bit for the Conditional Write Inhibit bit (CWI) of the Interrupt Condition Register (ICR).
D4	LEMTC	**LINK ERROR MONITOR THRESHOLD COMPARISON:** The comparison bit for the Link Error Monitor Threshold bit (LEMT) of the Interrupt Condition Register (ICR).
D5	RCAC	**RECEIVE CONDITION A COMPARISON:** The comparison bit for the Receive Condition A bit (RCA) of the Interrupt Condition Register (ICR).
D6	RCBC	**RECEIVE CONDITION B COMPARISON:** The comparison bit for the Receive Condition B bit (RCB) of the Interrupt Condition Register (ICR).
D7	UDIC	**USER DEFINABLE INTERRUPT COMPARISON:** The comparison bit for the User Definable Interrupt bit (UDIC) of the Interrupt Condition Register (ICR).

5.28 CURRENT TRANSMIT STATE COMPARISON REGISTER (CTSCR)

The Current Transmit State Comparison Register ensures that the Control Bus must first read a bit modified by the PLAYER+ device before it can be written to by the Control Bus Interface.

The current state of the Current Transmit State Register (CTSR) is automatically written into the Current Transmit State Comparison Register A (i.e. CTSCR=CTSR) during a Control Bus Interface read cycle of CTSR.

During a Control Bus Interface write cycle, the PLAYER+ device will set the Conditional Write Inhibit bit (CWI) of the Interrupt Condition Register (ICR) to 1 and disallow the setting or clearing of a bit within the CTSR when the value of a bit in the CTSR differs from the value of the corresponding bit in the Current Transmit State Comparison Register.

ACCESS RULES

ADDRESS	READ	WRITE
1Bh	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
RESC	PRDPEC	SEC	IC1C	IC0C	TM2C	TM1C	TM0C

Bit	Symbol	Description
D0	TM0C	**TRANSMIT MODE <0> COMPARISON:** The comparison bit for the Transmit Mode <0> bit (TM0) of the Current Transmit State Register (CTSR).
D1	TM1C	**TRANSMIT MODE <1> COMPARISON:** The comparison bit for the Transmit Mode <1> bit (TM1) of the Current Transmit State Register (CTSR).
D2	TM2C	**TRANSMIT MODE <2> COMPARISON:** The comparison bit for the Transmit Mode <2> bit (TM2) of the Current Transmit State Register (CTSR).
D3	IC0C	**INJECTION CONTROL <0> COMPARISON:** The comparison bit for the Injection Control <0> bit (IC0) of the Current Transmit State Register (CTSR).
D4	IC1C	**INJECTION CONTROL <1> COMPARISON:** The comparison bit for the Injection Control <1> bit (IC1) of the Current Transmit State Register (CTSR).
D5	SEC	**SMOOTHER ENABLE COMPARISON:** The comparison bit for the Smoother Enable bit (SE) of the Current Transmit State Register (CTSR).
D6	PRDPEC	**PHY__REQUEST DATA PARITY ENABLE COMPARISON:** The comparison bit for the PHY__Request Data Parity Enable bit (PRDPE) of the Current Transmit State Register (CTSR).
D7	RESC	**RESERVED COMPARISON:** The comparison bit for the Reserved bit (RES) of the Current Transmit State Register (CTSR).

5.0 Registers (Continued)

5.29 RECEIVE CONDITION COMPARISON REGISTER A (RCCRA)

The Receive Condition Comparison Register A ensures that the Control Bus must first read a bit modified by the PLAYER+ device before it can be written to by the Control Bus Interface.

The current state of RCRA is automatically written into the Receive Condition Comparison Register A (i.e. RCCRA=RCRA) during a Control Bus Interface read cycle of RCRA.

During a Control Bus Interface write cycle, the PLAYER+ device will set the Conditional Write Inhibit bit (CWI) of the Interrupt Condition Register (ICR) to 1 and prevent the setting or clearing of a bit within RCRA when the value of a bit in RCRA differs from the value of the corresponding bit in the Receive Condition Comparison Register A.

ACCESS RULES

ADDRESS	READ	WRITE
1Ch	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
LSUPIC	LSCC	NTC	NLSC	MLSC	HLSC	QLSC	NSDC

Bit	Symbol	Description
D0	NSDC	**NO SIGNAL DETECT COMPARISON:** The comparison bit for the No Signal Detect bit (NSD) of the Receive Condition Register A (RCRA).
D1	QLSC	**QUIET LINE STATE COMPARISON:** The comparison bit for the Quiet Line State bit (QLS) of the Receive Condition Register A (RCRA).
D2	HLSC	**HALT LINE STATE COMPARISON:** The comparison bit for the Halt Line State bit (HLS) of the Receive Condition Register A (RCRA).
D3	MLSC	**MASTER LINE STATE COMPARISON:** The comparison bit for the Master Line State bit (MLS) of the Receive Condition Register A (RCRA).
D4	NLSC	**NOISE LINE STATE COMPARISON:** The comparison bit for the Noise Line State bit (NLS) of the Receive Condition Register A (RCRA).
D5	NTC	**NOISE THRESHOLD COMPARISON:** The comparison bit for the Noise Threshold bit (NT) of the Receive Condition Register A (RCRA).
D6	LSCC	**LINE STATE CHANGE COMPARISON:** The comparison bit for the Line State Change bit (LSC) of the Receive Condition Register A (RCRA).
D7	LSUPIC	**LINE STATE UNKNOWN AND PHY INVALID COMPARISON:** The comparison bit for the Line State Unknown and PHY Invalid bit (LSUPI) of the Receive Condition Register A (RCRA).

5.30 RECEIVE CONDITION COMPARISION REGISTER B (RCCRB)

The Receive Condition Comparison Register B ensures that the Control Bus must first read a bit modified by the PLAYER+ device before it can be written to by the Control Bus Interface.

The current state of RCRB is automatically written into the Receive Condition Comparison Register B (i.e. RCCRB = RCRB) during a Control Bus Interface read cycle RCRB.

During a Control Bus Interface write cycle, the PLAYER+ device will set the Conditional Write Inhibit bit (CWI) of the Interrupt Condition Register (ICR) to 1 and prevent the setting or clearing of a bit within RCRB when the value of a bit in RCRB differs from the value of the corresponding bit in the Receive Condition Comparison Register B.

ACCESS RULES

ADDRESS	READ	WRITE
1Dh	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
RESC	SILSC	EBOUC	CSEC	LSUPVC	ALSC	STC	ILSC

Bit	Symbol	Description
D0	ILSC	**IDLE LINE STATE COMPARISON:** The comparison bit for the Idle Line State bit (ILS) of the Receive Condition Register B (RCRB).
D1	STC	**STATE THRESHOLD COMPARISON:** The comparison bit for the State Threshold bit (ST) of the Receive Condition Register B (RCRB).
D2	ALSC	**ACTIVE LINE STATE COMPARISON:** The comparison bit for the Active Line State bit (ALS) of the Receive Condition Register B (RCRB).
D3	LSUPVC	**LINE STATE UNKNOWN AND PHY VALID COMPARISON:** The comparison bit for the Line State Unknown and PHY Valid bit (LSUPV) of the Receive Condition Register B (RCRB).
D4	CSEC	**CONNECTION SERVICE EVENT COMPARISON / CASCADE SYNCHRONIZATION ERROR:** The comparison bit for the Cascade Synchronization Error/Connection Service Event bit (CSE) of the Receive Condition Register B (RCRB).
D5	EBOUC	**ELASTICITY BUFFER OVERFLOW / UNDERFLOW COMPARISON:** The comparison bit for the Elasticity Buffer Overflow/Underflow bit (EBOU) of the Receive Condition Register B (RCRB).
D6	SILSC	**SUPER IDLE LINE STATE COMPARISON:** The comparison bit for the Super Idle Line State bit (SILS) of the Receive Condition Register B (RCRB).
D7	RESC	**RESERVED COMPARISON:** The comparison bit for the Reserved bit (RES) of the Receive Condition Register B (RCRB).

5.0 Registers (Continued)

5.31 MODE REGISTER 2 (MODE2)

The Mode Register 2 (MODE2) is used to configure the PLAYER+ device.

The register is used to software reset the chip, setup data parity, and enable scrubbing functions.

Note: This register can not be written to during reset.

ACCESS RULES

ADDRESS	READ	WRITE
1Eh	Always	Conditional

D7	D6	D5	D4	D3	D2	D1	D0
ESTC	RES	CLKSEL	RES	RES	RES	CBPE	PHYRST

Bit	Symbol	Description
D0	PHYRST	**PLAYER RESET:** This bit can be used as a master software reset of the PLAYER function within the PLAYER+ device. The clock distribution and recovery sections of the chip are not affected by this reset. The PLAYER+ automatically clears this bit 32 byte time after its assertion to indicate that the reset action has been completed. This bit can be set through a C-Bus write, but can only be cleared by the PLAYER+.
D1	CBPE	**C-Bus Parity Enable:** This bit disables or enables parity checking on C-Bus data. When this bit is set to 0, no parity checking is done. When the bit is set to 1, parity checking is enabled during a C-Bus write cycle. Should a mismatch occur, the C-Bus Data Parity Error (ICR.CPE) bit will be set and the corresponding C-Bus access is discarded. C-Bus data parity is always generated during a C-Bus read cycle.
D2–D4	RES	**RESERVED:** Reserved for future use.
D5	CLKSEL	**CLOCK SELECT:** This bit controls the frequency of the CLK16 output. It resets to 0 which sets the CLK16 output to a 15.625 MHz frequency. When set to 1 a 31.25 MHz frequency is generated. **Note:** When the value of this bit is changed, no glitches appear on the CLK16 output due to the frequency change.
D6	RES	**RESERVED:** Reserved for future use.
D7	ESTC	**ENABLE SCRUBBING on TRIGGER CONDITIONS:** When ESTC is set to 1 and a Trigger Condition occurs (as set in the TDR register), the Trigger Transition Configuration Register (TTCR) is loaded into the Configuration Register (CR) and scrubbing is started on all indicate ports that have changed. Scrubbing is accomplished by sending out 2 Phy_Invalid symbols followed by "scrub"symbol pairs for a time defined by the Scrub Timer Threshold register.

5.0 Registers (Continued)

5.32 CMT CONDITION COMPARISON REGISTER (CMTCCR)

The CMT Condition Comparison Register (CMTCR) ensures that the Control Bus must first read a bit modified by the PLAYER+ device before it can be written to by the Control Bus Interface.

The current state of the CMT Condition Register (CMTCR) is automatically written into the CMT Condition Comparison Register (CMTCR) (i.e. CMTCCR = CMTCR) during a Control Bus Interface read-cycle of CMTCR.

During a Control Bus Interface write cycle, the PLAYER+ device will set the Conditional Write Inhibit bit (CWI) of the Interrupt Control Register (ICR) to 1 and disallow the setting or clearing of a bit within the CMTCR when the value of a bit in the CMTCR differs from the value of the corresponding bit in the CMT Condition Comparison Register.

ACCESS RULES

ADDRESS	READ	WRITE
1Fh	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
TCOC	STEC	RES	RES	RES	RES	RES	RES

Bit	Symbol	Description
D0-D5	RES	**RESERVED:** Reserved for future use.
D6	STEC	**SCRUB TIMER EXPIRED COMPARISON:** The comparison bit for the Scrub Timer Expire bit (STE) of the CMT Condition Register (CMTCR).
D7	TCOC	**TRIGGER CONDITION OCCURRED COMPARISON:** The comparison bit for the Trigger Condition Occurred (TCO) bit of the CMT Condition Register (CMTCR).

5.0 Registers (Continued)

5.33 CMT CONDITION REGISTER (CMTCR)

The CMT Condition Register maintains a history of all CMT events and actions performed. The corresponding CMT Condition Mask Register (CMTCMR) can be used to generate an interrupt. When the bits in both the CMTCMR and CMTCR are set, the Receive Condition Register B's Connection Service Event (RCRB.CSE) bit will be set.

ACCESS RULES

ADDRESS	READ	WRITE
20h	Always	Conditional

D7	D6	D5	D4	D3	D2	D1	D0
TCO	STE	RES	RES	RES	RES	RES	RES

Bit	Symbol	Description
D0-D5	RES	**RESERVED:** Reserved for future use.
D6	STE	**SCRUB TIMER EXPIRED:** This bit is set to 1 when the Scrub Timer expires. **Note:** When STE is set, the Configuration Register (CR) is protected.
D7	TCO	**TRIGGER CONDITION OCCURRED:** This bit is set to 1 when a trigger condition is met. When a trigger occurs, the values in the Trigger Transmit Mode (TDR.TTM2-0) are loaded into the Current Transmit Mode Register (CTSR.TM2-0). **Note:** When TCO is set, the Current Transmit State Register (CTSR) is protected.

5.34 CMT CONDITION MASK REGISTER (CMTCMR)

This is the mask register for the CMT Condition Register (CMTCR). When the bits in both the CMTCMR and CMTCR are set, the Receive Condition Register B's Connection Service Event (RCRB.CSE) bit will be set.

ACCESS RULES

ADDRESS	READ	WRITE
21h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
TCOM	STEM	RES	RES	RES	RES	RES	RES

Bit	Symbol	Description
D0-D5	RES	**RESERVED:** Reserved for future use.
D6	STEM	**SCRUB TIMER EXPIRED MASK:** The mask bit for the Scrub Timer Expired (STE) bit of the CMT Condition Register (CMTCR).
D7	TCOM	**TRIGGER CONDITION OCCURRED MASK:** The mask bit for the Trigger Condition Occurred (TCO) bit of the CMT Condition Register (CMTCR).

5.0 Registers (Continued)

5.35 RESERVED REGISTERS 22H–23H (RR22H–RR23H)

This register is reserved for future use.

DO NOT ACCESS THIS REGISTER

ACCESS RULES

ADDRESS	READ	WRITE
22h–23h	Always	DO NOT WRITE

5.36 SCRUB TIMER THRESHOLD REGISTER (STTR)

This is the threshold value of the internal scrub timer. It has a resolution of 40.96 μs and a maximum value of ~10 ms. When the scrub timer reaches zero, the Scrub Timer Expired (CMTCR.STE) bit is set.

Scrubbing is initiated when MODE2.ESTC = 1 and a trigger condition occurs.

Writing to STTR during scrubbing will not affect the scrubbing action.

ACCESS RULES

ADDRESS	READ	WRITE
24h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
STT7	STT6	STT5	STT4	STT3	STT2	STT1	STT0

Bit	Symbol	Description
D0–D7	STT0–STT7	**SCRUB TIMER THRESHOLD BIT<0-7>:** Scrub Timer threshold. STT0 is the Least Significant Bit (LSB).

5.37 SCRUB TIMER VALUE REGISTER (STVR)

This is a snap-shot of the current value of the upper 8 bits of the scrub timer.

During a Control Bus Interface write cycle, the Control Bus Write Command Reject bit (CCR) of the Interrupt Condition Register (ICR) will be set to 1 and will ignore a write cycle.

ACCESS RULES

ADDRESS	READ	WRITE
25h	Always	Write Reject

D7	D6	D5	D4	D3	D2	D1	D0
STV7	STV6	STV5	STV4	STV3	STV2	STV1	STV0

Bit	Symbol	Description
D0–D7	STV0–STV7	**SCRUB TIMER VALUE BIT <0-7>:** Snap-shot of the scrub timer. STV0 is the Least Significant Bit (LSB).

5.38 TRIGGER DEFINITION REGISTER (TDR)

This register determines which events cause a trigger transition and which transmit mode is entered when a trigger transition is detected. The trigger transmit modes are the same as those found in the Current Transmit State Register (CTSR), and are loaded from the TDR into the CTSR when any of the selected trigger conditions occur. When a trigger condition occurs CMTCR.TCO is set.

The Trigger Definition Register is useful to implement the strict PC_React time requirement.

ACCESS RULES

ADDRESS	READ	WRITE
26h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
TONT	TOQLS	TOHLS	TOMLS	TOSILS	TTM2	TTM1	TTM0

Bit	Symbol	Description
D0, D1, D2	TTM0, TTM1, TTM2	**TRIGGER TRANSMIT MODE <0, 1, 2>:** These bits select one of 6 transmission modes to be loaded into the Current Transmit State Register (CTSR) when a trigger condition is detected. The trigger condition is selected by the upper 5 bits of this register.
D3	TOSILS	**TRIGGER ON SILS:** Trigger when SILS is received.
D4	TOMLS	**TRIGGER ON MLS:** Trigger when MLS is received.
D5	TOHLS	**TRIGGER ON HLS:** Trigger when HLS is received.
D6	TOQLS	**TRIGGER ON QLS (or NSD):** Trigger when QLS is received.
D7	TONT	**TRIGGER ON Noise Threshold:** Trigger when Noise Threshold is reached (Current Noise Register = 0).

TTM2	TTM1	TTM0	
0	0	0	**Active Transmit Mode (ATM):** Normal transmission of incoming PHY Request data.
0	0	1	**Idle Transmit Mode (ITM):** Transmission of Idle symbol pairs (11111 11111).
0	1	0	**Off Transmit Mode (OTM):** Transmission of Quiet symbol pairs (00000 00000) and deassertion of the PMD transmitter Enable pin (TXE).
0	1	1	**Reserved:** Reserved for future use. Users are discouraged from using this transmit mode. If selected, however, the transmitter will generate Quiet symbol pairs (00000 00000).
1	0	0	**Master Transmit Mode (MTM):** Transmission of Halt and Quiet symbol pairs (00100 00000).
1	0	1	**Halt Transmit Mode (HTM):** Transmission of Halt symbol pairs (00100 00100).
1	1	0	**Quiet Transmit Mode (QTM):** Transmission of Quiet symbol pairs (00000 00000).
1	1	1	**Reserved:** Reserved for future use. Users are discouraged from using this transmit mode. If selected, however, the transmitter will generate Quiet symbol pairs (00000 00000).

5.0 Registers (Continued)

5.39 TRIGGER TRANSITION CONFIGURATION REGISTER (TTCR)

The Trigger Transition Configuration Register holds the configuration switch setting to be loaded into the Configuration Register (CR) when a trigger transition takes place. When scrubbing is enabled, scrubbing is performed for a period of time indicated by the Scrub Timer Threshold Register (STTR).The register bit descriptions for the Configuration Register and, therefore, the Trigger Transition Configuration Register are reprinted below.

ACCESS RULES

ADDRESS	READ	WRITE
27h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
BIE	AIE	TRS1	TRS0	BIS1	BIS0	AIS1	AIS0

Bit	Symbol	Description
D0, D1	AIS0, AIS1	**A_INDICATE SELECTOR <0, 1>:** The A_Indicate Selector <0, 1> bits selects one of the four Configuration Switch data buses for the A_Indicate output port (AIP, AIC, AID<7:0>). **AIS1 AIS0** 0 0 PHY Invalid Bus 0 1 Receiver Bus 1 0 A_Request Bus 1 1 B_Request Bus
D2, D3	BIS0, BIS1	**B_INDICATE SELECTOR <0, 1>:** The B_Indicate Selector <0, 1> bits selects one of the four Configuration Switch data buses for the B_Indicate output port (BIP, BIC, BID<7:0>). **BIS1 BIS0** 0 0 PHY Invalid Bus 0 1 Receiver 1 0 A_Request Bus 1 1 B_Request Bus **Note:** Even though this bit can be set and/or cleared in the DP83256 (for single path stations), it will not affect any I/Os since the DP83256 does not offer a B_Indicate port.
D4, D5	TRS0, TRS1	**TRANSMIT REQUEST SELECTOR <0, 1>:** The Transmit Request Selector <0, 1> bits selects one of the four Configuration Switch data buses for the input to the Transmitter Block. **TRS1 TRS0** 0 0 PHY Invalid Bus 0 1 Receiver Bus 1 0 A_Request Bus 1 1 B_Request Bus **Note:** If the PLAYER+ device is in Active Transmit Mode (i.e. the Transmit Mode bits (TM<2:0>) of the Current Transmit State Register (CTSR) are set to 000) and the PHY Invalid Bus is selected, then the PLAYER+ device will transmit continuous Idle symbols due to the Repeat Filter.
D6	AIE	**A_INDICATE ENABLE:** 0: Disables the A_Indicate output port. The A_Indicate port pins will be tri-stated when the port is disabled. 1: Enables the A_Indicate output port (AIP, AIC, AID<7:0>).
D7	BIE	**B_INDICATE ENABLE:** 0: Disables the B_Indicate output port. The B_Indicate port pins will be tri-stated when the port is disabled. 1: Enables the B_Indicate output port (BIP, BIC, BID<7:0>). **Note:** Even though this bit can be set and/or cleared in the DP83256 (for single path stations), it will not affect any I/Os since the DP83256 does not offer a B_Indicate port.

5.40 RESERVED REGISTERS 28H-3AH (RR28H-RR3AH)

These registers are reserved for future use.

DO NOT ACCESS THESE REGISTERS

ACCESS RULES

ADDRESS	READ	WRITE
28h–3Ah	Always	DO NOT WRITE

5.0 Registers (Continued)

5.41 CLOCK GENERATION MODULE REGISTER (CGMREG)

This register is used to enable or disable the 125 MHz ECL Transmit clock outputs. These outputs are not required for use in a standard FDDI board implementation and are disabled by default to reduce high frequency noise.

These TXC outputs are included for support of alternate FDDI PMDs, such as unshielded twisted pair copper cable.

DO NOT WRITE TO RESERVED REGISTER BITS. Writes to reserved register bits could prevent proper device operation. Therefore, read the register first, and then write it back with the non-reserved bits set to the desired value.

ACCESS RULES

ADDRESS	READ	WRITE
3Bh	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
RES	RES	FLTREN	RES	TXCE	RES	RES	RES

Bit	Symbol	Description
D0-D2	RES	**RESERVED BITS:** DO NOT CHANGE THE VALUE OF THESE BITS. Changes to reserved register bits could prevent proper device operation.
D3	TXCE	**TRANSMIT CLOCK ENABLE:** When bit is set to 1, 125 MHz ECL TXC outputs are enabled. When this bit is reset to 0, TXC outputs are disabled. TXC outputs are disabled on reset. **Note:** TXC clocks are only available on the 160-pin DP83257 PLAYER+ device.
D4	RES	**RESERVED BITS:** DO NOT CHANGE THE VALUE OF THESE BITS. Changes to reserved register bits could prevent proper device operation.
D5	FLTREN	**FILTER ENABLE:** When bit is set to 1, the internal loop filter node is connected to the LPFLTR pin for diagnostic viewing. This bit is reset to 0 by default, which disconnects the filter node from the LPFLTR pin. **Note:** In normal operation this bit should be disabled (=0).
D6-D7	RES	**RESERVED BITS:** DO NOT CHANGE THE VALUE OF THESE BITS. Changes to reserved register bits could prevent proper device operation.

5.42 ALTERNATE PMD REGISTER (APMDREG)

This register is used to enable or disable the Alternate PMD inputs and ouputs. These signals are not required for use in FDDI board implementations that do not require a scrambler that is external to the PLAYER+ device. The actual interface consists of the signal pairs RXC_OUT, RXD_OUT, RXC_IN, and RXD_IN.

The interface is disabled by default and should only be enabled if it is being used.

DO NOT WRITE TO RESERVED REGISTER BITS. Writes to reserved register bits could prevent proper device operation. Therefore, read the register first, and then write it back with the non-reserved bits set to the desired value.

Note: The Alternate PMD Interface pins are only available on the 160-pin DP83257 PLAYER+ device. The Alternate PMD Interface is disabled on reset.

ACCESS RULES

ADDRESS	READ	WRITE
3Ch	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
RES	RES	RES	RES	APMDEN	RES	RES	RES

Bit	Symbol	Description
D0–D2	RES	**RESERVED BITS:** DO NOT CHANGE THE VALUE OF THESE BITS. Changes to reserved register bits could prevent proper device operation.
D3	APMDEN	**ALTERNATE PMD ENABLE:** When bit is set to 1, the Alternate PMD Interface is enabled. When this bit is reset to 0, the Alternate PMD Interface is disabled. The Alternate PMD Interface consists of the following extra ECL signal pairs RXC_OUT, RXD_OUT, RXC_IN, and RXD_IN. In some alternate PMD implementations it may also be necessary to use the 125 MHz Transmit Clock signals (TXC). The TXC outputs must be separately enabled by the TXCE bit in the CGMREG register. **Note:** The Alternate PMD Interface pins are only available on the 160-pin DP83257 PLAYER+ device. The Alternate PMD Interface is disabled on reset.
D4–D7	RES	**RESERVED BITS:** DO NOT CHANGE THE VALUE OF THESE BITS. Changes to reserved register bits could prevent proper device operation.

5.43 RESERVED REGISTERS 3DH-3FH (RR3DH-RR3FH)

These registers are reserved for future use.

DO NOT ACCESS THESE REGISTERS

ACCESS RULES

ADDRESS	READ	WRITE
3Dh–3Fh	Always	DO NOT WRITE

6.0 Signal Descriptions

6.1 DP83256VF PIN DESCRIPTIONS

The pin descriptions for the DP83256VF are divided into 5 functional interfaces: PMD Interface, PHY Port Interface, Control Bus Interface, Clock Interface, and Miscellaneous Interface.

For a Pinout Summary list, refer to Table 8-1 and *Figure 8-1*, DP83256VF 100-Pin JEDEC Metric PQFP Pinout.

PMD INTERFACE

The PMD Interface consists of I/O signals used to connect the PLAYER+ device to the Physical Medium Dependant (PMD) sublayer.

Symbol	Pin #	I/O	Description
PMID+ PMID−	39 38	I	**PMD Indicate Data:** Differential, 100k ECL, 125 Mbps serial data input signals from the PMD receiver.
PMRD+ PMRD−	33 32	O	**PMD Request Data:** Differential, 100k ECL, 125 Mbps serial data output signals to the PMD transmitter.
SD+ SD−	37 36	I	**Signal Detect:** Differential 100k ECL input signals from the PMD receiver indicating that a signal is being received by the PMD receiver.
TEL	47	I	**PMD Transmitter Enable Level:** A TTL input signal to select the PMD transmitter Enable (TXE) signal level.
TXE	46	O	**PMD Transmitter Enable:** A TTL output signal to enable/disable the PMD transmitter. The output level of the TXE pin is determined by three parameters: the Transmit Enable (TE) bit in the Mode Register, the TM2-TM0 bits in the Current Transmit State Register, and the input to the TEL pin. The following rules summarize the output of the TXE pin: 1. If TE = 0 and TEL = GND, then TXE = V_{CC} 2. If TE = 0 and TEL = V_{CC}, then TXE = GND 3. If TE = 1 and OTM and TEL = GND, then TXE = V_{CC} 4. If TE = 1 and OTM and TEL = V_{CC}, then TXE = GND 5. If TE = 1 and not OTM and TEL = GND, then TXE = GND 6. If TE = 1 and not OTM and TEL = V_{CC}, then TXE = V_{CC}

6.0 Signal Descriptions (Continued)

PHY PORT INTERFACE

The PHY Port Interface consists of I/O signals used to connect the PLAYER+ device to the Media Access Control (MAC) sublayer or other PLAYER+ device. The DP83256 Device has two PHY Port Interfaces. The A__Indicate path from one PHY Port Interface and the B__Request path from the second PHY Port Interface. Each path consists of an odd parity bit, a control bit, and two 4-bit symbols.

Refer to section 3.3, the Configuration Switch, for more information.

Symbol	Pin #	I/O	Description
AIP	6	O	**PHY Port A Indicate Parity:** A TTL output signal representing odd parity for the 10-bit wide Port A Indicate signals (AIP, AIC, and AID<7:0>).
AIC	7	O	**PHY Port A Indicate Control:** TTL output signal indicating that the two 4-bit symbols (AID<7:4> and AID<3:0>) are either control symbols (AIC=1) or data symbols (AIC=0).
AID7 AID6 AID5 AID4	8 9 10 13	O	**PHY Port A Indicate Data:** TTL output signals representing the first 4-bit data/control symbol. AID7 is the most significant bit and AID4 is the least significant bit of the first symbol.
AID3 AID2 AID1 AID0	14 15 16 17	O	**PHY Port A Indicate Data:** TTL output signals representing the second 4-bit data/control symbol. AID3 is the most significant bit and AID0 is the least significant bit of the second symbol.
BRP	70	I	**PHY Port B Request Parity:** A TTL input signal representing odd parity for the 10-bit wide Port A Request signals (BRP, BRC, and BRD<7:0>).
BRC	69	I	**PHY Port B Request Control:** A TTL input signal indicating that the two 4-bit symbols (BRD<7:4> and BRD<3:0>) are either control symbols (BRC=1) or data symbols (BRC=0).
BRD7 BRD6 BRD5 BRD4	68 67 66 63	I	**PHY Port B Request Data:** TTL input signals representing the first 4-bit data/control symbol. BRD7 is the most significant bit and BRD4 is the least significant bit of the first symbol.
BRD3 BRD2 BRD1 BRD0	62 61 60 59	I	**PHY Port B Request Data:** TTL input signals representing the second 4-bit data/control symbol. BRD3 is the most significant bit and BRD0 is the least significant bit of the second symbol.

6.0 Signal Descriptions (Continued)

CONTROL BUS INTERFACE

The Control Bus Interface consists of I/O signals used to connect the PLAYER+ device to Station Management (SMT).

The Control Bus is an asynchronous interface between the PLAYER+ device and a general purpose microprocessor or other controller. It provides access to 64 8-bit internal registers.

In the PLAYER+ device the Control Bus address range has been expanded by 1-bit to 6 bits of address space.

Symbol	Pin #	I/O	Description
~CE	73	I	**Control Enable:** An active-low, TTL, input signal which enables the Control Bus port for a read or write cycle. R/~W, CBA<5:0>, CBP, and CBD<7:0> must be valid at the time ~CE is low.
R/~W	72	I	**Read/~Write:** A TTL input signal which indicates a read Control Bus cycle(R/~W=1), or a write Control Bus cycle (R/~W=0).
~ACK	75	O	**~Acknowledge:** An active low, TTL, open drain output signal which indicates the completion of a read or write cycle. During a read cycle, CBD<7:0> are valid as long as ~ACK is low (~ACK=0). During a write cycle, a microprocessor must hold CBD<7:0> valid until ~ACK becomes low. Once ~ACK is low, it will remain low as long as ~CE remains low (~CE=0).
~INT	74	O	**~Interrupt:** An active low, open drain, TTL, output signal indicating that an interrupt condition has occurred. The Interrupt Condition Register (ICR) should be read in order to find out the source of the interrupt. Interrupts can be masked through the use of the Interrupt Condition Mask Register (ICMR).
CBA5 CBA4 CBA3 CBA2 CBA1 CBA0	83 82 81 80 77 76	I	**Control Bus Address:** TTL input signals used to select the address of the register to be read or written. CBA5 is the most significant bit (MSB) and CBA0 is the least significant bit (LSB) of the address signals.
CBP	96	I/O	**Control Bus Parity:** A bidirectional, TTL signal representing odd parity for the Control Bus data (CBD<7:0>). During a read cycle, the signal is held valid by the PLAYER+ device as long as ~ACK is low. During a write cycle, the signal must be valid when ~CE is low, and must be held valid until ~ACK becomes low. If incorrect parity is used during a write cycle, the PLAYER+ device will inhibit the write cycle and set the Control Bus Data Parity Error (CPE) bit in the Interrupt Condition Register (ICR).
CBD7 CBD6 CBD5 CBD4 CBD3 CBD2 CBD1 CBD0	95 94 93 92 91 90 89 86	I/O	**Control Bus Data:** Bidirectional, TTL signals containing the data to be read from or written to a register. During a read cycle, the signal is held valid by the PLAYER+ device as long as ~ACK is low. During a write cycle, the signal must be valid when ~CE is low, and must be held valid until ~ACK becomes low.

6.0 Signal Descriptions (Continued)

CLOCK INTERFACE

The Clock Interface consists of 12.5 MHz and 25 MHz clocks supplied by the PLAYER+ device as well as reference and feedback inputs.

Symbol	Pin #	I/O	Description
LBC1 LBC2 LBC3 LBC4 LBC5	4 3 2 1 100	O	**Local Byte Clock:** TTL compatible, 12.5 MHz, 50% duty cycle clock outputs which are phase locked to a crystal oscillator or reference signal. The PH_SEL input determines whether the five phase outputs are phase offset by 8 ns or 16 ns.
PH_SEL	22	I	**Phase Select:** TTL compatible input used to select either a 8 ns or 16 ns phase offset between the 5 local byte clocks (LBC's). The LBC's are phase offset 8ns apart when PH_SEL is at a logic LOW level and 16 ns apart when at a logic HI level.
FBK_IN	25	I	**Feedback Input:** TTL compatible input for use as the PLL's phase comparator feedback input to close the Phase Locked Loop. This input is intended to be driven from one of the Local Byte Clocks (LBC's) from the same PLAYER+ device.
LSC	99	O	**Local Symbol Clock:** TTL compatible 25 MHz output for driving the MACSI or BMAC devices. This output's negative phase transition is aligned with the LBC1 output transitions and has a 40% HI and 60% LOW duty cycle.
CLK16	5	O	**Clock 16/32:** TTL compatible clock with a selectable frequency of approximately 15.625 MHz or 31.25 MHz. The frequency can be selected using the Clock Select (CLKSEL) bit of the Mode 2 Register (MODE2). **Note:** No glitches appear at the output when switching frequencies.
XTAL_IN	27	I	**External Crystal Oscillator Input:** This input in conjunction with the XTAL_OUT output, is designed for use of an external crystal oscillator network as the frequency reference for the clock generation module's internal VCO. A diagram of the required circuit, which includes only a 12.5 MHz crystal and 2 loading capacitors, is shown in *Figure 3-19*. This input is selected when the REF_SEL input is at a logic LOW level. When not being used, this input should be tied to ground.
XTAL_OUT	26	O	**External Crystal Oscillator Output:** This output in conjunction with the XTAL_IN input, is designed for use of an external crystal oscillator network as the frequency reference for the clock generation module's internal VCO. A diagram of the required circuit, which includes only a 12.5 MHz crystal and 2 loading capacitors, is shown in *Figure 3-19*.
REF_IN	24	I	**Reference Input:** TTL compatible input for use as the PLL's phase comparator reference frequency. This input is for use in dual attach station or concentrator configurations where there are multiple PLAYER+ devices at a given site requiring synchronization. This input is selected when the REF_SEL input is at a logic HI level.
REF_SEL	23	I	**Reference Select:** TTL compatible input which selects either the crystal oscillator inputs XTAL_IN and XTAL_OUT or the REF_IN inputs as the reference frequency inputs for the PLL. The crystal oscillator inputs are selected when REF_SEL is at a logic LOW level and the REF_IN input is selected as the reference when REF_SEL is at a logic HI level.
LPFLTR	30	O	**Loop Filter:** This is a diagnostic output that allows monitoring of the clock generation module's filter node. This output is disabled by default and does not need to be connected to any external device. It can be enabled using the FLTREN bit of the Clock generation module register (CGMREG). **Note:** In normal operation this pin should be disabled.

6.0 Signal Descriptions (Continued)

MISCELLANEOUS INTERFACE

The Miscellaneous Interface consist of a reset signal, user definable sense signals, and user definable enable signals.

Symbol	Pin #	I/O	Description
~RST	71	I	**Reset:** An active low, TTL, input signal which clears all registers. The signal must be kept asserted for a minimum amount of time. Once the ~RST signal is asserted, the PLAYER+ device should be allowed the specified amount of time to reset internal logic. Note that bit zero of the Mode Register will be set to zero (i.e. Stop Mode). See section 4.2, Stop Mode of Operation for more information
SP0	40	I	**User Definable Sense Pin 0:** A TTL input signal from a user defined source. Sense Bit 0 (SB0) of the User Definable Register (UDR) will be set to one if the signal is asserted for a minimum of 160 ns. Once the asserted signal is latched, Sense Bit 0 can only be cleared through the Control Bus Interface, even if the signal is deasserted. This ensures that the Control Bus Interface will record the source of events which can cause interrupts.
SP1	42	I	**User Definable Sense Pin 1:** A TTL input signal from a user defined source. Sense Bit 1 (SB1) of the User Definable Register (UDR) will be set to one if the signal is asserted for a minimum of 160 ns. Once the asserted signal is latched, Sense Bit 1 can only be cleared through the Control Bus Interface, even if the signal is deasserted. This ensures that the Control Bus Interface will record the source of events which can cause interrupts.
EP0	41	O	**User Definable Enable Pin 0:** A TTL output signal allowing control of external logic through the Control Bus Interface. EP0 is asserted/deasserted through Enable Bit 0 (EB0) of the User Definable Register (UDR). When Enable Bit 0 is set to zero, EP0 is deasserted. When Enable Bit 0 is set to one, EP0 is asserted.
EP1	43	O	**User Definable Enable Pin 1:** A TTL output signal allowing control of external logic through the Control Bus Interface. EP1 is asserted/deasserted through Enable Bit 1 (EB1) of the User Definable Register (UDR). When Enable Bit 1 is set to zero, EP1 is deasserted. When Enable Bit 1 is set to one, EP1 is asserted.

6.0 Signal Descriptions (Continued)

POWER AND GROUND

All power pins should be connected to a single +5V power supply. All ground pins should be connected to a common 0V ground supply. Bypassing and filtering requirements are given in a separate User Information Document.

Symbol	Pin #	I/O	Description
V_{CC}_CORE	88		**Power:** Positive 5V power supply for the core PLAYER section logic gates.
GND_CORE	87		**Ground:** Power supply return for the core PLAYER section logic gates.
V_{CC}_ECL	20, 31, 34, 44, 56,		**Power:** Positive 5V power supply for the PLAYER+ device's ECL logic gates.
GND_ECL	21, 35, 45, 55		**Ground:** Power supply return for the PLAYER+ device's ECL logic gates.
V_{CC}_ESD	28		**Power:** Positive 5V power supply for the PLAYER+ device's ESD protection circuitry.
GND_ESD	29		**Ground:** Power supply return for the PLAYER+ device's ESD protection circuitry.
V_{CC}_IO	11, 65, 79, 98		**Power:** Positive 5V power supply for the input/output buffers.
GND_IO	12, 64, 78, 97		**Ground:** Power supply return for the input/output buffers.

SPECIAL CONNECT PINS

These are pins that have special connection requirements.

No Connect (N/C) pins should not be connected to anything. This means not to power, not to ground, and not to each other.

Reserved_0 (RES_0) pins must be connected to ground. These pins are not used to supply device power so they do not need to be filtered or bypassed.

Reserved_1 (RES_1) pins must be connected to power. These pins are not used to supply device power so they do not need to be filtered or bypassed.

Symbol	Pin #	I/O	Description
N/C	49, 54		**No Connect:** Pins should not be connected to anything. This means not to power, not to ground, and not to each other.
RES_0	18, 19, 48, 50, 51, 52, 53, 57, 58, 84		**Reserved 0:** Pins must be connected to ground. These pins are not used to supply device power so they do not need to be filtered or bypassed.
RES_1	85		**Reserved 1:** Pins must be connected to power. These pins are not used to supply device power so they do not need to be filtered or bypassed.

6.0 Signal Descriptions (Continued)

6.2 DP83257VF SIGNAL DESCRIPTIONS

The pin descriptions for the DP83257VF are divided into five functional interfaces; PMD Interface, PHY Port Interface, Control Bus Interface, Clock Interface, and Miscellaneous Interface.

For a Pinout Summary List, refer to Table 8-2 and *Figure 8-2*, DP83257VF 160-Pin JEDEC Metric PQFP Pinout.

PMD INTERFACE

The PMD Interface consists of I/O signals used to connect the PLAYER+ device to the Physical Medium Dependant (PMD) sublayer.

The DP83257 PLAYER+ device actually has two PMD interfaces. The Primary PMD Interface and the Alternate PMD Interface.

The Primary PMD Interface should be used for all PMD implementations that do not require an external scrambler/descrambler function, clock recovery function, or clock generation function, such as a Fiber Optic or Shielded Twisted Pair (SDDI) PMD. The second, Alternate PMD Interface can be used to support Unshielded Twisted Pair (UTP) PMDs that require external scrambling, with no external clock recovery or clock generation functions required.

Section 3.8 describes how the PLAYER+ can be connected to the PMD and how the Alternate PMD can be enabled.

Note that when the Alternate PMD Interface is not being used, the pins that make up the interface must be connected in the specific way described in the following Alternate PMD Interface table.

Primary PMD Interface

Symbol	Pin #	I/O	Description
PMID+ PMID−	62 61	I	**PMD Indicate Data:** Differential, 100k ECL, 125 Mbps serial data input signals from the PMD Receiver into the Clock Recovery Module (CRM) of the PLAYER+.
PMRD+ PMRD−	54 53	O	**PMD Request Data:** Differential, 100k ECL, 125 Mbps serial data output signals to the PMD transmitter.
SD+ SD−	60 59	I	**Signal Detect:** Differential 100k ECL input signals from the PMD receiver indicating that a signal is being received by the PMD receiver.
TEL	74	I	**PMD Transmitter Enable Level:** A TTL input signal to select the PMD transmitter Enable (TXE) signal level.
TXE	73	O	**PMD Transmitter Enable:** A TTL output signal to enable/disable the PMD transmitter. The output level of the TXE pin is determined by three parameters: the Transmit Enable (TE) bit in the Mode Register, the TM2–TM0 bits in the Current Transmit State Register, and the input to the TEL pin. The following rules summarize the output of the TXE pin: 1. If TE = 0 and TEL = GND, then TXE = V_{CC} 2. If TE = 0 and TEL = V_{CC}, then TXE = GND 3. If TE = 1 and OTM and TEL = GND, then TXE = V_{CC} 4. If TE = 1 and OTM and TEL = V_{CC}, then TXE = GND 5. If TE = 1 and not OTM and TEL = GND, then TXE = GND 6. If TE = 1 and not OTM and TEL = V_{CC}, then TXE = V_{CC}

6.0 Signal Descriptions (Continued)

Alternate PMD Interface

Symbol	Pin #	I/O	Description
PMID+ PMID−	62 61	I	**PMD Indicate Data:** Differential, 100k ECL, 125 Mbps serial data input signals from the PMD Receiver into the Clock Recovery Module (CRM) of the PLAYER+.
RXC_OUT+ RXC_OUT−	56 55	O	**Recovered Clock Out:** 125 MHz clock recovered by the Clock Recovery Module (CRM) from the PMID data input. These signals are only active when the Alternate PMD Enable (APMDEN) bit of the Alternate PMD Register (APMDREG) is set to a 1 and are off by default after Reset. When these two pins are not used they should be left Not Connected (N/C).
RXD_OUT+ RXD_OUT−	83 82	O	**Recovered Data Out:** 125 Mbps data recovered by the Clock Recovery Module (CRM) from the PMID data input. These signals are only active when the Alternate PMD Enable (APMDEN) bit of the Alternate PMD Register (APMDREG) is set to a 1 and are off by default after Reset. When these two pins are not used they should be left Not Connected (N/C).
RXC_IN+ RXC_IN−	76 75	I	**Receive Clock In:** Clock inputs to the Player section of the PLAYER+. These inputs must be synchronized with the RXD_IN inputs. These signals are only active when the Alternate PMD Enable (APMDEN) bit of the Alternate PMD Register (APMDREG) is set to a 1 and are off by default after Reset. When these two pins are not used, pin 76 should be left Not Connected (N/C) and pin 75 should be connected directly to ground (Reserved_0).
RXD_IN+ RXD_IN−	78 77	I	**Receive Data In:** Data inputs to the Player section of the PLAYER+. These inputs must be synchronized with the RXC_IN inputs. These signals are only active when the Alternate PMD Enable (APMDEN) bit of the Alternate PMD Register (APMDREG) is set to a 1 and are off by default after Reset. When these two pins are not used, pin 78 should be left Not Connected (N/C) and pin 77 should be connected directly to ground (Reserved_0).
PMRD+ PMRD−	54 53	O	**PMD Request Data:** Differential, 100k ECL, 125 Mbps serial data output signals to the PMD transmitter.
TXC+ TXC−	51 50	O	**Transmit Clock:** 125 MHz, 100k ECL compatible differential outputs synchronized to the outgoing PMRD data. These signals can be enabled using the Transmit Clock Enable (TXCE) bit in the Clock Generation Module Register (CGMREG). When these two pins are not used they should be left Not Connected (N/C).
SD+ SD−	60 59	I	**Signal Detect:** Differential, 100k ECL, input signals from the PMD receiver indicating that a signal is being received by the PMD receiver.
TEL	74	I	**PMD Transmitter Enable Level:** A TTL input signal to select the PMD transmitter Enable (TXE) signal level.
TXE	73	O	**PMD Transmitter Enable:** A TTL output signal to enable/disable the PMD transmitter. The output level of the TXE pin is determined by three parameters: the Transmit Enable (TE) bit in the Mode Register, the TM2–TM0 bits in the Current Transmit State Register, and the input to the TEL pin. The following rules summarize the output of the TXE pin: 1. If TE = 0 and TEL = GND, then TXE = V_{CC} 2. If TE = 0 and TEL = V_{CC}, then TXE = GND 3. If TE = 1 and OTM and TEL = GND, then TXE = V_{CC} 4. If TE = 1 and OTM and TEL = V_{CC}, then TXE = GND 5. If TE = 1 and not OTM and TEL = GND, then TXE = GND 6. If TE = 1 and not OTM and TEL = V_{CC}, then TXE = V_{CC}

6.0 Signal Descriptions (Continued)

PHY PORT INTERFACE

The PHY Port Interface consists of I/O signals used to connect the PLAYER+ device to the Media Access Control (MAC) sublayer or other PLAYER+ device. The DP83257 Device has two PHY Port Interfaces. The A_Request and A_Indicate paths from one PHY Port Interface and the B_Request and B_Indicate paths from the second PHY Port Interface. Each path consists of an odd parity bit, a control bit, and two 4-bit symbols.

Refer to section 3.3, the Configuration Switch, for more information.

Symbol	Pin #	I/O	Description
AIP	6	O	**PHY Port A Indicate Parity:** A TTL output signal representing odd parity for the 10-bit wide Port A Indicate signals (AIP, AIC, and AID<7:0>).
AIC	8	O	**PHY Port A Indicate Control:** A TTL output signal indicating that the two 4-bit symbols (AID<7:4> and AID<3:0>) are either control symbols (AIC=1) or data symbols (AIC=0).
AID7 AID6 AID5 AID4	10 12 14 18	O	**PHY Port A Indicate Data:** TTL output signals representing the first 4-bit data/control symbol. AID7 is the most significant bit and AID4 is the least significant bit of the first symbol.
AID3 AID2 AID1 AID0	20 22 24 26	O	**PHY Port A Indicate Data:** TTL output signals representing the second 4-bit data/control symbol. AID3 is the most significant bit and AID0 is the least significant bit of the second symbol.
ARP	7	I	**PHY Port A Request Parity:** A TTL input signal representing odd parity for the 10-bit wide Port A Request signals (ARP, ARC, and ARD<7:0>).
ARC	9	I	**PHY Port A Request Control:** A TTL input signal indicating that the two 4-bit symbols (ARD<7:4> and ARD<3:0>) are either control symbols (ARC=1) or data symbols (ARC=0).
ARD7 ARD6 ARD5 ARD4	11 13 15 19	I	**PHY Port A Request Data:** TTL input signals representing the first 4-bit data/control symbol. ARD7 is the most significant bit and ARD4 is the least significant bit of the first symbol.
ARD3 ARD2 ARD1 ARD0	21 23 25 27	I	**PHY Port A Request Data:** TTL input signals representing the second 4-bit data/control symbol. ARD3 is the most significant bit and ARD0 is the least significant bit of the second symbol.
BIP	114	O	**PHY Port B Indicate Parity:** A TTL output signal representing odd parity for the 10-bit wide Port A Indicate signals (BIP, BIC, and BID<7:0>).
BIC	112	O	**PHY Port B Indicate Control:** A TTL output signal indicating that the two 4-bit symbols (BID<7:4> and BID<3:0>) are either control symbols (BIC=1) or data symbols (BIC=0).
BID7 BID6 BID5 BID4	110 108 106 102	O	**PHY Port B Indicate Data:** TTL output signals representing the first 4-bit data/control symbol. BID7 is the most significant bit and BID4 is the least significant bit of the first symbol.
BID3 BID2 BID1 BID0	100 98 96 94	O	**PHY Port B Indicate Data:** TTL output signals representing the second 4-bit data/control symbol. BID3 is the most significant bit and BID0 is the least significant bit of the second symbol.
BRP	115	I	**PHY Port B Request Parity:** A TTL input signal representing odd parity for the 10-bit wide Port A Request signals (BRP, BRC, and BRD<7:0>).
BRC	113	I	**PHY Port B Request Control:** A TTL input signal indicating that the two 4-bit symbols (BRD<7:4> and BRD<3:0>) are either control symbols (BRC=1) or data symbols (BRC=0).

6.0 Signal Descriptions (Continued)

Symbol	Pin #	I/O	Description
BRD7 BRD6 BRD5 BRD4	111 109 107 103	I	**PHY Port B Request Data:** TTL input signals representing the first 4-bit data/control symbol. BRD7 is the most significant bit and BRD4 is the least significant bit of the first symbol.
BRD3 BRD2 BRD1 BRD0	101 99 97 95	I	**PHY Port B Request Data:** TTL input signals representing the second 4-bit data/control symbol. BRD3 is the most significant bit and BRD0 is the least significant bit of the second symbol.

6.0 Signal Descriptions (Continued)

CONTROL BUS INTERFACE

The Control Bus Interface consists of I/O signals used to connect the PLAYER+ device to Station Management (SMT).

The Control Bus is an asynchronous interface between the PLAYER+ device and a general purpose microprocessor or other controller. It provides access to 64 8-bit internal registers.

In the PLAYER+ device the Control Bus address range has been expanded by 1-bit to 6 bits of address space.

Symbol	Pin #	I/O	Description
~CE	118	I	**Control Enable:** An active-low, TTL, input signal which enables the Control Bus port for a read or write cycle. R/~W, CBA<5:0>, CBP, and CBD<7:0> must be valid at the time ~CE is low.
R/~W	117	I	**Read/~Write:** A TTL input signal which indicates a read Control Bus cycle (R/~W=1), or a write Control Bus cycle (R/~W=0).
~ACK	120	O	~**Acknowledge:** An active low, TTL, open drain output signal which indicates the completion of a read or write cycle. During a read cycle, CBD<7:0> are valid as long as ~ACK is low (~ACK=0). During a write cycle, a microprocessor must hold CBD<7:0> valid until ~ACK becomes low. Once ~ACK is low, it will remain low as long as ~CE remains low (~CE=0).
~INT	119	O	~**Interrupt:** An active low, open drain, TTL, output signal indicating that an interrupt condition has occurred. The Interrupt Condition Register (ICR) should be read in order to find out the source of the interrupt. Interrupts can be masked through the use of the Interrupt Condition Mask Register (ICMR).
CBA5 CBA4 CBA3 CBA2 CBA1 CBA0	135 134 133 132 129 128	I	**Control Bus Address:** TTL input signals used to select the address of the register to be read or written. CBA5 is the most significant bit (MSB) and CBA0 is the least significant bit (LSB) of the address signals.
CBP	148	I/O	**Control Bus Parity:** A bidirectional, TTL signal representing odd parity for the Control Bus data (CBD>7:0>). During a read cycle, the signal is held valid by the PLAYER+ device as long as ~ACK is low. During a write cycle, the signal must be valid when ~CE is low, and must be held valid until ~ACK becomes low. If incorrect parity is used during a write cycle, the PLAYER+ device will inhibit the write cycle and set the Control Bus Data Parity Error (CPE) bit in the Interrupt Condition Register (ICR).
CBD7 CBD6 CBD5 CBD4 CBD3 CBD2 CBD1 CBD0	147 146 145 144 143 142 141 138	I/O	**Control Bus Data:** Bidirectional, TTL signals containing the data to be read from or written to a register. During a read cycle, the signal is held valid by the PLAYER+ device as long as ~ACK is low. During a write cycle, the signal must be valid when ~CE is low, and must be held valid until ~ACK becomes low.

6.0 Signal Descriptions (Continued)

CLOCK INTERFACE

The Clock Interface consists of 12.5 MHz and 25 MHz clocks supplied by the PLAYER+ device as well as reference and feedback inputs.

Symbol	Pin #	I/O	Description
LBC1 LBC2 LBC3 LBC4 LBC5	4 3 2 1 160	O	**Local Byte Clock:** TTL compatible, 12.5 MHz, 50% duty cycle clock outputs which are phase locked to a crystal oscillator or reference signal. The PH_SEL input determines whether the five phase outputs are phase offset by 8 ns or 16 ns.
PH_SEL	34	I	**Phase Select:** TTL compatible input used to select either a 8 ns or 16 ns phase offset between the 5 local byte clocks (LBC's). The LBC's are phase offset 8 ns apart when PH_SEL is at a logic LOW level and 16 ns apart when at a logic HI level.
FBK_IN	37	I	**Feedback Input:** TTL compatible input for use as the PLL's phase comparator feedback input to close the Phase Locked Loop. This input is intended to be driven from one of the Local Byte Clocks (LBC's) from the same PLAYER+ device.
LSC	159	O	**Local Symbol Clock:** TTL compatible 25 MHz output for driving the MACSI or BMAC devices. This output's negative phase transition is aligned with the LBC1 output transitions and has a 40% HI and 60% LOW duty cycle.
CLK16	5	O	**Clock 16/32:** TTL compatible clock with a selectable frequency of approximately 15.625 MHz or 31.25 MHz. The frequency can be selected using the Clock Select (CLKSEL) bit of the Mode 2 Register (MODE2). **Note:** No glitches appear at the output when switching frequencies.
XTAL_IN	46	I	**External Crystal Oscillator Input:** This input in conjunction with the XTAL_OUT output, is designed for use of an external crystal oscillator network as the frequency reference for the clock generation module's internal VCO. A diagram of the required circuit, which includes only a 12.5 MHz crystal and 2 loading capacitors, is shown in *Figure 3-19*. This input is selected when the REF_SEL input is at a logic LOW level. When not being used, this input should be tied to ground.
XTAL_OUT	45	O	**External Crystal Oscillator Output:** This output in conjunction with the XTAL_IN input, is designed for use of an external crystal oscillator network as the frequency reference for the clock generation module's internal VCO. A diagram of the required circuit, which includes only a 12.5 MHz crystal and 2 loading capacitors, is shown in *Figure 3-19*.
REF_IN	36	I	**Reference Input:** TTL compatible input for use as the PLL's phase comparator reference frequency. This input is for use in dual attach station or concentrator configurations where there are multiple PLAYER+ devices at a given site requiring synchronization. This input is selected when the REF_SEL input is at a logic HI level.
REF_SEL	35	I	**Reference Select:** TTL compatible input which selects either the crystal oscillator inputs XTAL_IN and XTAL_OUT or the REF_IN inputs as the reference frequency inputs for the PLL. The crystal oscillator inputs are selected when REF_SEL is at a logic LOW level and the REF_IN input is selected as the reference when REF_SEL is at a logic HI level.
LPFLTR	49	O	**Loop Filter:** This is a diagnostic output that allows monitoring of the clock generation module's filter node. This output is disabled by default and does not need to be connected to any external device. It can be enabled using the FLTREN bit of the Clock generation module register (CGMREG). **Note:** In normal operation this pin should be disabled.

6.0 Signal Descriptions (Continued)

MISCELLANEOUS INTERFACE

The Miscellaneous Interface consist of a reset signal, user definable sense signals, and user definable enable signals.

Symbol	Pin #	I/O	Description
~RST	116	I	**Reset:** An active low, TTL, input signal which clears all registers. The signal must be kept asserted for a minimum amount of time. Once the ~RST signal is asserted, the PLAYER+ device should be allowed the specified amount of time to reset internal logic. Note that bit zero of the Mode Register will be set to zero (i.e. Stop Mode). See section 4.2, Stop Mode of Operation for more information
SP0	63	I	**User Definable Sense Pin 0:** A TTL input signal from a user defined source. Sense Bit 0 (SB0) of the User Definable Register (UDR) will be set to one if the signal is asserted for a minimum of 160 ns. Once the asserted signal is latched, Sense Bit 0 can only be cleared through the Control Bus Interface, even if the signal is deasserted. This ensures that the Control Bus Interface will record the source of events which can cause interrupts.
SP1	65	I	**User Definable Sense Pin 1:** A TTL input signal from a user defined source. Sense Bit 1 (SB1) of the User Definable Register (UDR) will be set to one if the signal is asserted for a minimum of 160 ns. Once the asserted signal is latched, Sense Bit 1 can only be cleared through the Control Bus Interface, even if the signal is deasserted. This ensures that the Control Bus Interface will record the source of events which can cause interrupts.
SP2	67	I	**User Definable Sense Pin 2:** A TTL input signal from a user defined source. Sense Bit 2 (SB2) of the User Definable Register (UDR) will be set to one if the signal is asserted for a minimum of 160 ns. Once the asserted signal is latched, Sense Bit 2 can only be cleared through the Control Bus Interface, even if the signal is deasserted. This ensures that the Control Bus Interface will record the source of events which can cause interrupts.
EP0	64	O	**User Definable Enable Pin 0:** A TTL output signal allowing control of external logic through the Control Bus Interface. EP0 is asserted/deasserted through Enable Bit 0 (EB0) of the User Definable Register (UDR). When Enable Bit 0 is set to zero, EP0 is deasserted. When Enable Bit 0 is set to one, EP0 is asserted.
EP1	66	O	**User Definable Enable Pin 1:** A TTL output signal allowing control of external logic through the Control Bus Interface. EP1 is asserted/deasserted through Enable Bit 1 (EB1) of the User Definable Register (UDR). When Enable Bit 1 is set to zero, EP1 is deasserted. When Enable Bit 1 is set to one, EP1 is asserted.
EP2	68	O	**User Definable Enable Pin 2:** A TTL output signal allowing control of external logic through the Control Bus Interface. EP2 is asserted/deasserted through Enable Bit 2 (EB2) of the User Definable Register (UDR). When Enable Bit 2 is set to zero, EP2 is deasserted. When Enable Bit 2 is set to one, EP2 is asserted.
CS	69	I	**Cascade Start:** A TTL input signal used to synchronize cascaded PLAYER+ devices in point-to-point applications. The signal is asserted when all of the cascaded PLAYER+ devices have the Cascade Mode (CM) bit of the Mode Register (MR) set to one, and all of the Cascade Ready (CR) pins of the cascaded PLAYER+ devices have been released. For further information, refer to section 4.4, Cascade Mode of Operation.
CR	70	O	**Cascade Ready:** An Open Drain output signal used to synchronize cascaded PLAYER+ devices in point-to-point applications. The signal is released (i.e. an Open Drain line is released) when all the cascaded PLAYER+ devices have the Cascade Mode (CM) bit of the Mode Register (MR) is set to one and a JK symbol pair has been received. For further information, refer to section 4.4, Cascade Mode of Operation.

6.0 Signal Descriptions (Continued)

POWER AND GROUND

All power pins should be connected to a single +5V power supply. All ground pins should be connected to a common 0V ground supply. Bypassing and filtering requirements are given in a separate User Information Document.

Symbol	Pin #	I/O	Description
V_{CC}_CORE	140		**Power:** Positive 5V power supply for the core PLAYER logic gates.
GND_CORE	139		**Ground:** Power supply return for the core PLAYER logic gates.
V_{CC}_ECL	32, 52, 57, 71, 89		**Power:** Positive 5V power supply for the PLAYER+ device's ECL logic gates.
GND_ECL	33, 58, 72, 88		**Ground:** Power supply return for the PLAYER+ device's ECL logic gates.
V_{CC}_ESD	47		**Power:** Positive 5V power supply for the PLAYER+ device's ESD protection circuitry.
GND_ESD	48		**Ground:** Power supply return for the PLAYER+ device's ESD protection circuitry.
V_{CC}_IO	16, 105, 131, 158		**Power:** Positive 5V power supply for the input/output buffers.
GND_IO	17, 104, 130, 157		**Ground:** Power supply return for the input/output buffers.

SPECIAL CONNECT PINS

These are pins that have special connection requirements.

No Connect (N/C) pins should not be connected to anything. This means not to power, not to ground, and not to each other.

Reserved_0 (RES_0) pins must be connected to ground. These pins are not used to supply device power so they do not need to be filtered or bypassed.

Reserved_1 (RES_1) pins must be connected to power. These pins are not used to supply device power so they do not need to be filtered or bypassed.

Symbol	Pin #	I/O	Description
N/C	38, 39, 40, 41, 42, 43, 44, 79, 80, 81, 87, 121, 122, 123, 124, 125, 126, 127, 149, 150, 151, 152, 153,154, 155, 156		**No Connect:** Pins should not be connected to anything. This means not to power, not to ground, and not to each other.
RES_0	28, 29, 30, 31, 84, 85, 86, 90, 91, 92, 93, 136		**Reserved 0:** Pins must be connected to ground. These pins are not used to supply device power so they do not need to be filtered or bypassed.
RES_1	137		**Reserved 1:** Pins must be connected to power. These pins are not used to supply device power so they do not need to be filtered or bypassed.

7.0 Electrical Characteristics

7.1 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC}	Supply Voltage		−0.5		7.0	V
DC_{IN}	Input Voltage		−0.5		V_{CC} + 0.5	V
DC_{OUT}	Output Voltage		−0.5		V_{CC} + 0.5	V
	Storge Temperature		−65		150	°C
ECL	Signal Output Current		−50			mA
	ESD Protection		2000			V

7.2 RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC}	Supply Voltage		4.75		5.25	V
T_A	Operating Temperature			25		°C
FREF	Reference Input Frequency		12.5−50 ppm	12.5	12.5 + 50 ppm	MHz
XTAL	Crystal Specifications					
	Center Frequency			12.5		MHz
	Frequency Calibration		−20		20	ppm
	Frequency Stability	Over Temperature	−20		20	ppm
	Aging	Less Than	−10		10	ppm

7.3 DC ELECTRICAL CHARACTERISITCS

The DC characteristics are over the operating range, unless otherwise specified.

DC electrical characteristics for the TTL-compatible, TRI-STATE output signals of PHY Port Interface and Control Bus Interface.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OZ1}	TRI-STATE Leakage (CBP and CBD7−CBD0)	$V_{OUT} = V_{CC}$			10	μA
I_{OZ2}	TRI-STATE Leakage (CBP and CBD7−CBD0)	$V_{OUT} = V_{GND}$			−10	μA
I_{OZ3}	TRI-STATE Leakage (AID and BID)	$V_{OUT} = V_{CC}$ (Note 1)			60	μA
I_{OZ4}	TRI-STATE Leakage (AID and BID)	$V_{OUT} = V_{GND}$ (Note 1)			−500	μA

Note 1: Output buffer has a p-channel pullup device.

7.0 Electrical Characteristics (Continued)

DC electrical characteristics for all TTL-compatible input signals and the following TTL-compatible output signals: PMD transmitter Enable (TXE), Enable Pins (EPn).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	Output High Voltage	$I_{OH} = -2$ mA	$V_{CC} - 0.5$			V
V_{OL}	Output Low Voltage	$I_{OL} = 4$mA			0.5	V
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
V_{IC}	Input Clamp Voltage	$I_{IN} = -18$ mA			−1.5	V
I_{IL}	Input Low Current	$V_{IN} =$ GND			−10	μA
I_{IH}	Input High Current	$V_{IN} = V_{CC}$			+10	μA

DC electrical characteristics for all LSC and LBC signals:

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	Output High Voltage	$I_{OH} = -400$ μA	$V_{CC} - 2$			V
V_{OL}	Output Low Voltage	$I_{OL} = 8$ mA			0.5	V

DC electrical characteristics for all Open Drain outputs signals (~INT, ~ACK, and CR)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OL}	Output Low Voltage	$I_{OL} = 8$ mA			0.5	V
I_{OZ}	TRI-STATE Leakage	$V_{OUT} = V_{CC}$			10	μA

DC electrical characteristics for all ECL input and output signals (PMID, PMRD, SD)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	Output High Voltage	$V_{IN} = V_{IH}$ (max)		$V_{CC} - 0.95$		V
V_{OL}	Output Low Voltage	$V_{IN} = V_{IL}$ (min)		$V_{CC} - 1.70$		V
V_{IH}	Input High Voltage			$V_{CC} - 1.02$		V
V_{IL}	Input Low Voltage			$V_{CC} - 1.64$		V
I_{IL}	Input Low Current	$V_{IN} = V_{IL}$ (min)		100		μA
I_{IH}	Input High Current	$V_{IN} = V_{IH}$ (max)		100		μA

Supply Current electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Total Supply			250 (Note 1)		mA

Note 1: The PLAYER+ device has multiple pairs of differential ECL outputs that need to be terminated. The additional current needed for this termination is not included in the PLAYER+'s total supply current, but can be calculated as follows:

V_{OH}_max $= V_{CC} - 0.88V$

V_{OL}_max $= V_{CC} - 1.62V$

Since the outputs are differential, the average output level is $V_{CC} - 1.25V$. The test load per output is 50Ω at $V_{CC} - 2V$, therefore the external load current through the 50Ω resistor is:

$$I_{LOAD} = [(V_{CC} - 1.25) - (V_{CC} - 2)]/50$$
$$= 0.015A$$
$$= 15 \text{ mA}$$

As a result, the termination for each pair of active ECL outputs consumes 30 mA, time averaged.

7.0 Electrical Characteristics (Continued)

7.4 AC ELECTRICAL CHARACTERISTICS

The AC Electrical characteristics are over the operating range, unless otherwise specified.

AC Characteristics for the Control Bus Interface

Symbol	Descriptions	Min	Max	Units
T1	$\overline{CE}$ Setup to LBC	5		ns
T2	LBC Period	80		ns
T3	LBC1 to $\overline{ACK}$ Low		45	ns
T4	$\overline{CE}$ Low to $\overline{ACK}$ Low	290	540	ns
T5	LBC1 Low to CBD(7-0) and CBP Valid		60	ns
T6	LBC1 to CBD(7-0) and CBP Active	5	60	ns
T7	$\overline{CE}$ Low to CBD(7-0) and CBP Active	225	475	ns
T8	$\overline{CE}$ Low to CBD(7-0) and CBP Valid	265	515	ns
T9	LBC Pulse Width High	35	45	ns
T10	LBC Pulse Width Low	35	45	ns
T11	$\overline{CE}$ High to $\overline{ACK}$ High		45	ns
T12	R/$\overline{W}$, CBA(5-0), CBD(7-0) and CBP Setup to $\overline{CE}$ Low	5		ns
T13	$\overline{CE}$ High to R/W, CBA(5-0), CBD(7-0) and CBP Hold Time	0		ns
T14	R/$\overline{W}$, CBA(5-0), CBD(7-0) and CBP to LBC1 Setup Time	0		ns
T15	$\overline{ACK}$ Low to $\overline{CE}$ High Lead Time	0		ns
T16	$\overline{CE}$ Minimum Pulse Width High	10		ns
T17	$\overline{CE}$ High to CBD(7-0) and CBP TRI-STATE		55	ns
T18	$\overline{ACK}$ High to $\overline{CE}$ Low	0		ns
T19	CBD(7-0) Valid to $\overline{ACK}$ Low Setup	20		ns
T20a	LBC1 to R/$\overline{W}$ Hold Time	10		ns
T20b	LBC1 to CBA Hold Time	10		ns
T20c	LBC1 to CBD and CBP Hold Time	20		ns
T21	LBC1 to $\overline{INT}$ Low		55	ns
T22	LBC1 to $\overline{INT}$ High		60	ns

Asynchronous Definitions

T4 (min)	T1 + (3 * T2) + T3
T4 (max)	T1 + (6 * T2) + T3
T7 (min)	T1 + (2 * T2) + T6
T7 (max)	T1 + (5 * T2) + T6
T8 (min)	T1 + (2 * T2) + T9 + T5
T8 (max)	T1 + (5 * T2) + T9 + T5

Note: Min/Max numbers are based on T2 = 80 ns and T9 = T40 = 40 ns.

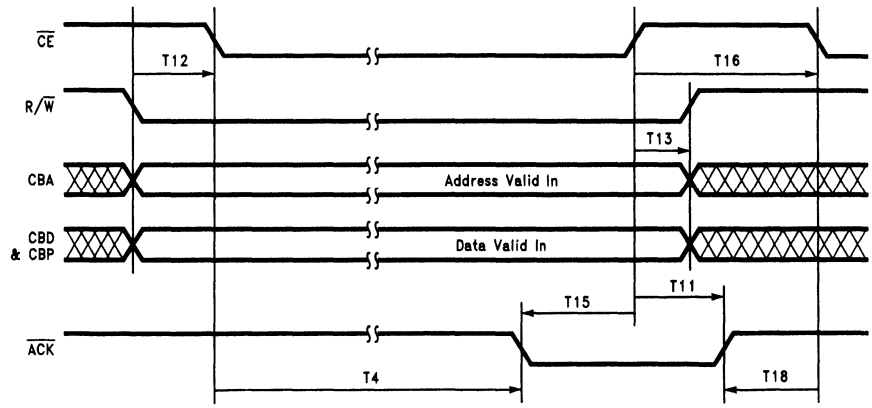

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FIGURE 7-1. Asynchronous Control Bus Write Cycle Timing

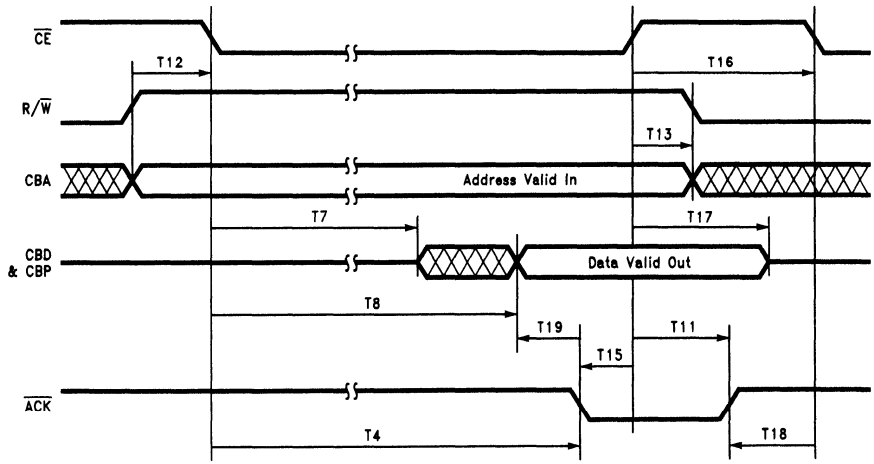

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FIGURE 7-2. Asynchronous Control Bus Read Cycle Timing

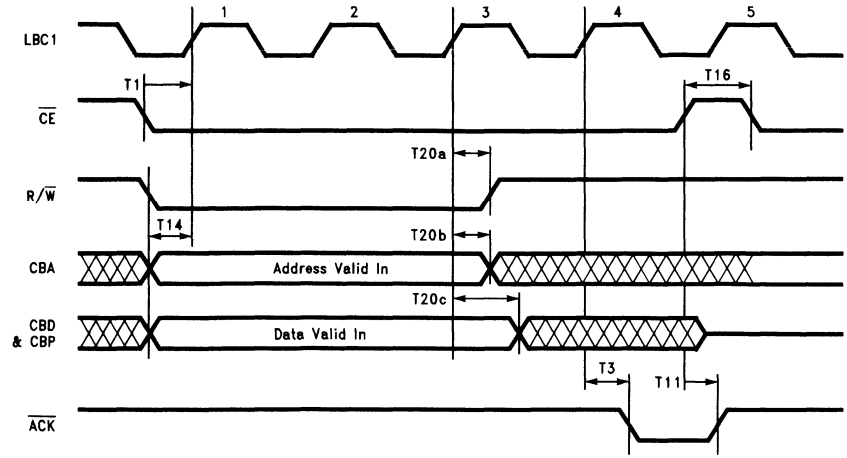

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FIGURE 7-3. Control Bus Synchronous Writes

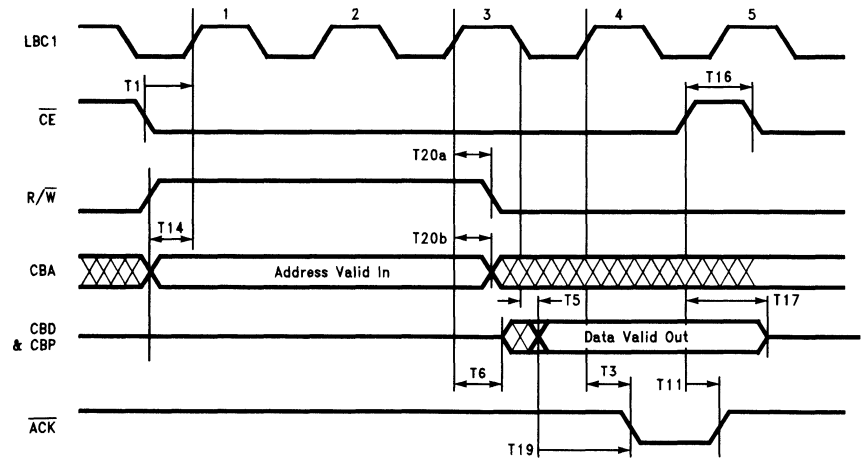

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FIGURE 7-4. Control Bus Synchronous Reads

7.0 Electrical Characteristics (Continued)

AC Characteristics for the Clock Interface Signals (Timing and Relationships)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{Phase1}	LBC1–LBC2 Timing	PH_SEL = LOW		8		ns
T_{Phase2}	LBC1–LBC3 Timing	PH_SEL = LOW		16		ns
T_{Phase3}	LBC1–LBC4 Timing	PH_SEL = LOW		24		ns
T_{Phase4}	LBC1–LBC5 Timing	PH_SEL = LOW		32		ns
T_{Phase1}	LBC1–LBC2 Timing	PH_SEL = HIGH		48		ns
T_{Phase2}	LBC1–LBC3 Timing	PH_SEL = HIGH		16		ns
T_{Phase3}	LBC1–LBC4 Timing	PH_SEL = HIGH		64		ns
T_{Phase4}	LBC1–LBC5 Timing	PH_SEL = HIGH		32		ns
T23	LSC to LBC1		−4		+6	ns
T24	REF_IN to FBK_IN	In Lock	−3		+3	ns

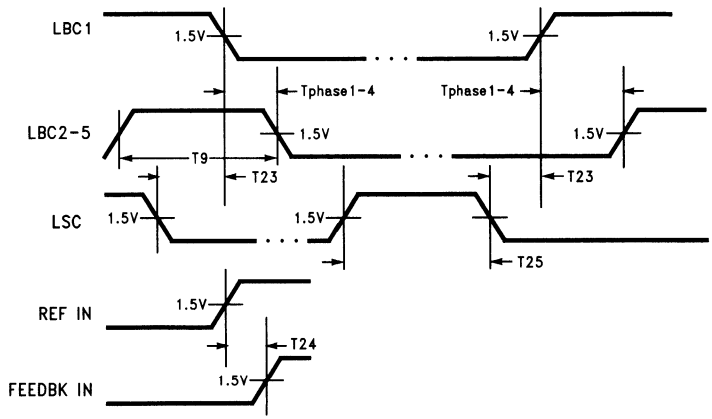

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FIGURE 7-5. Clock Signal Relationships

7.0 Electrical Characteristics (Continued)

AC Characteristics for the Clock Interface Signals (Periods and Pulse Widths)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T2	LBC Period			80		ns
T9	LBC Pulse Width High		35		45	ns
T10	LBC Pulse Width Low		35		45	ns
T25	LSC Pulse Width High		12		19	ns
T26	LSC Pulse Width Low		21		28	ns
T27	CLK16 Period	MODE2.CLKSEL = 0		64		ns
T28	CLK16 Pulse Width	MODE2.CLKSEL = 0		32		ns
T27	CLK16 Period	MODE2.CLKSEL = 1		32		ns
T28	CLK16 Pulse Width	MODE2.CLKSEL = 1		16		ns

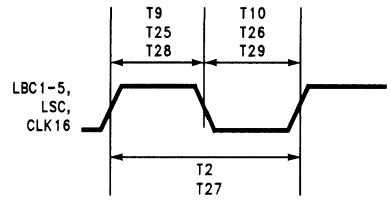

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FIGURE 7-6. Clock Pulse Widths

AC Characteristics for Port A Interface and Port B Interface

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T30	LBC1 to Indicate Data Changes from TRI-STATE to Valid Data				70	ns
T31	LBC1 to Indicate Data Changes from Active to TRI-STATE				70	ns
T32	LBC1 to Indicate Data Sustain		11			ns
T33	LBC1 to Valid Indicate Data				45	ns
T34	Request Data to LBC1 Setup Time		15			ns
T35	Request Data to LBC1 Hold Time		5			ns

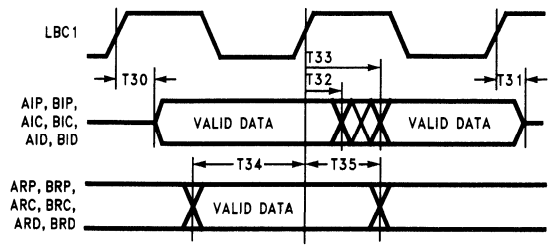

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FIGURE 7-7. PHY Port Interface Timing

7.0 Electrical Characteristics (Continued)

AC Characteristics for the PMD Interface

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T36	TXC to PMRD Change Time	(Note 2)			6	ns
T37	TXC Pulse Width High	(Notes 1, 2)		4		ns
T38	TXC Rise Time	(Notes 1, 2)			1.5	ns
T39	TXC Fall Time	(Notes 1, 2)			1.5	ns
T40	PMRD Rise Time			1.5		ns
T41	PMRD Fall Time			1.5		ns
T42	SD Minimum Pulse Width		120			ns

Note 1: This parameter is not directly tested but is guaranteed through correlation to device characterization data.

Note 2: TXC is only available on the 160 pin version of this part and must be activated by the CGM_REG.TXCE bit.

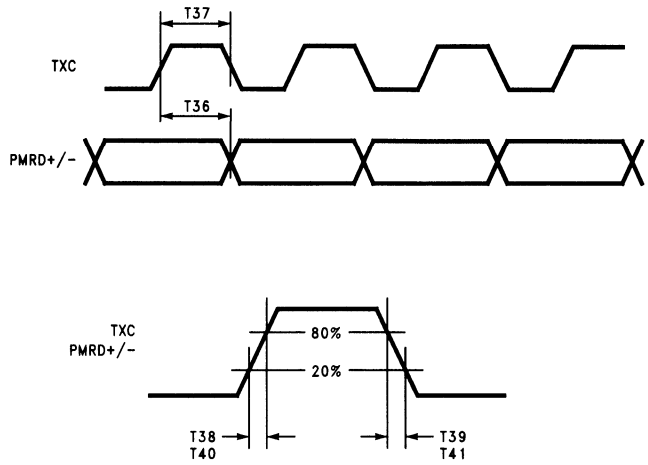

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FIGURE 7-8. PMRD Timing Diagrams

7.0 Electrical Characteristics (Continued)

AC Characteristics for the PMD Interface (ANSI Specifications) The Conditions Notes that are enclosed in square brackets contain the ANSI specification reference for the parameter.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	PMRD Duty Cycle Distortion (DCD)	(Note 2) [PMD 8.1]			1.0	ns p-p
	PMRD Data Dependent Jitter (DDJ)	(Note 2) [PMD 8.1]			0.6	ns p-p
	PMRD Random Jitter (RJ)	(Notes 1, 2) [PMD 8.1]			0.76	ns p-p
	CRM Data Recovery Window	[PMD E.2]	−3		3	ns
	CRM Receive Clock Tolerance (CRM Lock Acquisition Range) **Note:** The elasticity buffer may limit the total system range to a smaller value	(Note 2) [PHY 5.2.4]	−200		200	ppm
	Receive Clock Acquisition Time	(Note 2) from 1st Data [PHY 5.2.6]			100	μs
	Receive Clock Acquisition Time	(Note 2) from Line State Change [PHY 5.2.6]			15	μs
	Local Clock (TXC) Frequency	(Notes 2, 3) [PHY 5.2.7]	−0.005%	125	+0.005%	MHz
	TXC Phase Jitter (above 200 kHz)	(Notes 2, 3) [PHY 5.2.7]	−8		+8	Degrees

Note 1: A Peak-peak Random Jitter (RJ) components are evaluated at a probability of 2.5 x 10-10. For a Gaussian distribution, the peak-peak jitter is then 12.6 times the rms jitter.

Note 2: This parameter is not tested at this time.

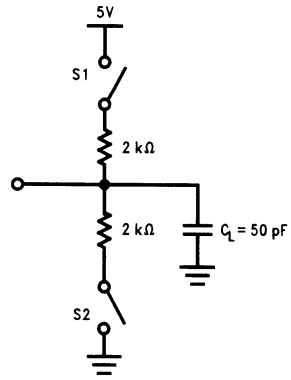
Note 3: TXC is only available on the 160 pin version of this part and must be activated by the CGM__REG.TXCE bit.

AC Characteristics for Miscellaneous Interface

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Minimum Reset (RST) Pulse Width			300		ns
	Maximum Reset Cycle Duration			10		ms
	Recommended Power Supply Bypassing Capacitor Value (**Note:** Capacitors should be placed between each supply pair as close to the device as possible.)			0.1		μF

7.0 Electrical Characteristics (Continued)

AC TEST CIRCUITS



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Note: S_1 is closed for T_{PZL} and T_{PLZ}
S_2 is closed for T_{PZH} and T_{PHZ}
S_1 and S_2 are open otherwise

FIGURE 7-10. Switching Test Circuit for All TRI-STATE Output Signals

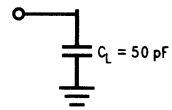

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FIGURE 7-11. Switching Test Circuit for All TTL Output Signals

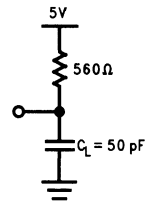

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FIGURE 7-12. Switching Test Circuit for All Open Drain Output Signals (INT, ACK, and CR)

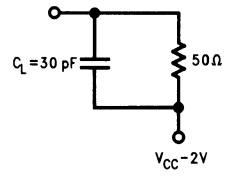

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FIGURE 7-13. Switching Test Circuit for All ECL Input and Output Signals

7.0 Electrical Characteristics (Continued)

TEST WAVEFORMS

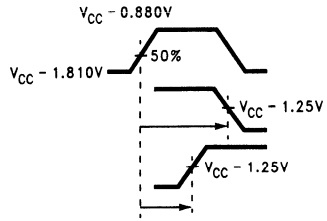

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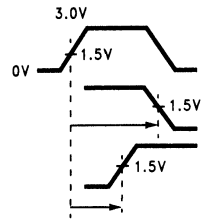
FIGURE 7-14. ECL Output Test Waveform



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Note: All CMOS Inputs and outputs are TTL compatible.

FIGURE 7-15. TTL Output Test Waveform

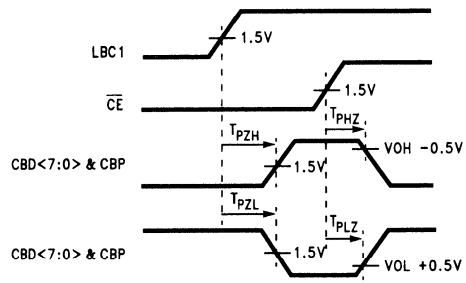

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FIGURE 7-16. TRI-STATE Output Test Waveform

8.0 Connection Diagrams

8.1 DP83256VF CONNECTION DIAGRAM

For a Pinout Summary List, refer to Table 8-1.

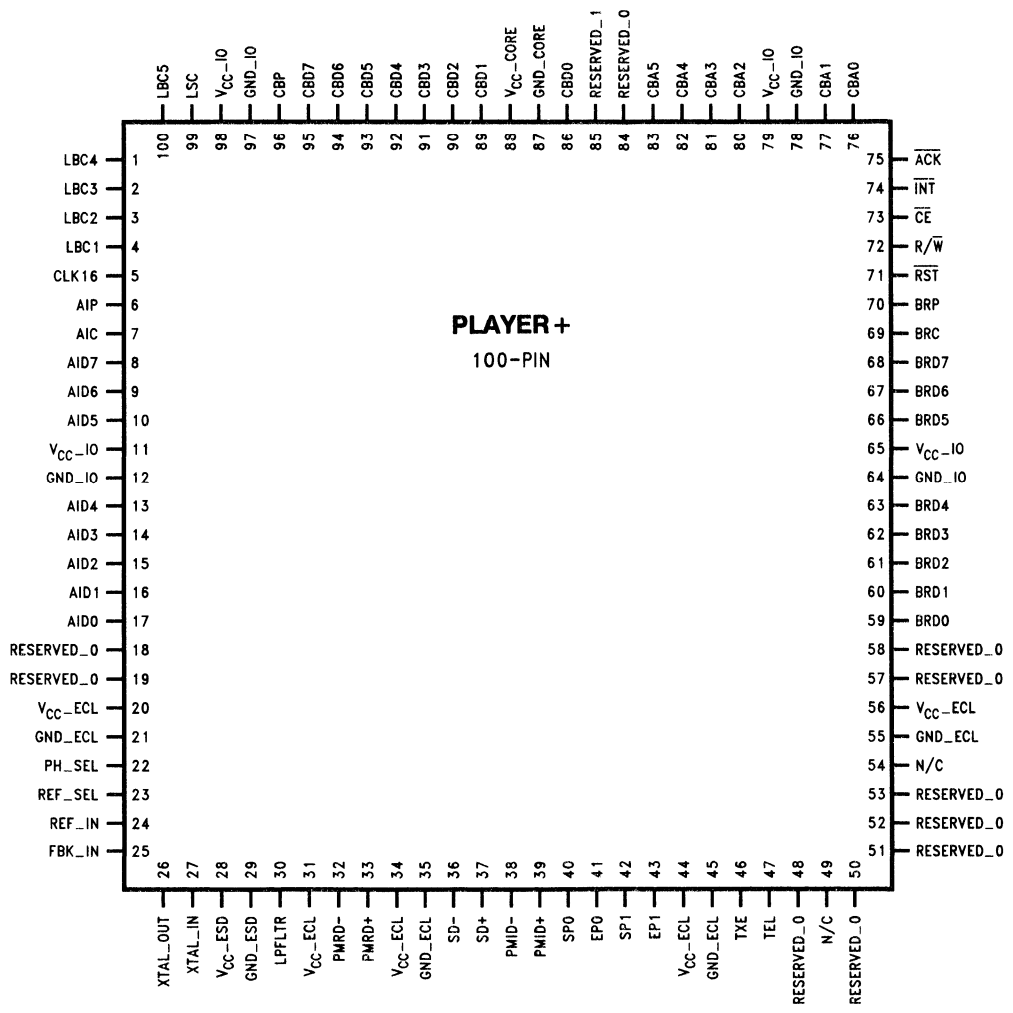

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FIGURE 8-1. DP83256VF 100-Pin JEDEC Metric PQFP Pinout

8.0 Connection Diagrams (Continued)

TABLE 8-1. DP83256 100-Pin PQFP Pinout Summary

Pin No.	Signal Name	Symbol	I/O	Pin Type
1	Local Byte Clock 4	LBC4	O	TTL
2	Local Byte Clock 3	LBC3	O	TTL
3	Local Byte Clock 2	LBC2	O	TTL
4	Local Byte Clock 1	LBC1	O	TTL
5	Clock 16/32	CLK16	O	TTL
6	PHY Port A Indicate Parity	AIP	O	TTL
7	PHY Port A Indicate Control	AIC	O	TTL
8	PHY Port A Indicate Data<7>	AID7	O	TTL
9	PHY Port A Indicate Data<6>	AID6	O	TTL
10	PHY Port A Indicate Data<5>	AID5	O	TTL
11	I/O Power	V_{CC}_IO		+5V
12	I/O Ground	GND_IO		+0V
13	PHY Port A Indicate Data<4>	AID4	O	TTL
14	PHY Port A Indicate Data<3>	AID3	O	TTL
15	PHY Port A Indicate Data<2>	AID2	O	TTL
16	PHY Port A Indicate Data<1>	AID1	O	TTL
17	PHY Port A Indicate Data<0>	AID0	O	TTL
18	Reserved_0	RES_0		+0V
19	Reserved_0	RES_0		+0V
20	ECL Power	V_{CC}_ECL		+5V
21	ECL Ground	GND_ECL		+0 V
22	Phase Select	PH_SEL	I	TTL
23	Reference Select	REF_SEL	I	TTL
24	Reference Input	REF_IN	I	TTL
25	Feedback Input	FBK_IN	I	TTL
26	Crystal Output	XTAL_OUT	O	
27	Crystal Input	XTAL_IN	I	
28	ESD Power	V_{CC}_ESD		+5V
29	ESD Ground	GND_ESD		+0V
30	Loop Filter	LPFLTR	O	
31	ECL Power	V_{CC}_ECL		+5V
32	PMD Request Data −	PMRD−	O	ECL
33	PMD Request Data +	PMRD+	O	ECL
34	ECL Power	V_{CC}_ECL		+5V
35	ECL Ground	GND_ECL		+0V
36	Signal Detect −	SD−	I	ECL
37	Signal Detect +	SD+	I	ECL
38	PMD Indicate Data −	PMID−	I	ECL

8.0 Connection Diagrams (Continued)

TABLE 8-1. DP83256 100-Pin PQFP Pinout Summary (Continued)

Pin No.	Signal Name	Symbol	I/O	Pin Type
39	PMD Indicate Data +	PMID+	I	ECL
40	Sense Pin 0	SP0	I	TTL
41	Enable Pin 0	EP0	O	TTL
42	Sense Pin 1	SP1	I	TTL
43	Enable Pin 1	EP1	O	TTL
44	ECL Power	V_{CC}_ECL		+5V
45	ECL Ground	GND_ECL		+0V
46	PMD Transmitter Enable	TXE	O	TTL
47	PMD Transmitter Enable Level	TEL	I	TTL
48	Reserved_0	RES_0		+0V
49	No Connect	N/C		
50	Reserved_0	RES_0		+0V
51	Reserved_0	RES_0		+0V
52	Reserved_0	RES_0		+0V
53	Reserved_0	RES_0		+0V
54	No Connect	N/C		
55	ECL Ground	GND_ECL		+0V
56	ECL Power	V_{CC}_ECL		+5V
57	Reserved_0	RES_0		+0V
58	Reserved_0	RES_0		+0V
59	PHY Port B Request Data<0>	BRD0	I	TTL
60	PHY Port B Request Data<1>	BRD1	I	TTL
61	PHY Port B Request Data<2>	BRD2	I	TTL
62	PHY Port B Request Data<3>	BRD3	I	TTL
63	PHY Port B Request Data<4>	BRD4	I	TTL
64	I/O Ground	GND_IO		+0V
65	I/O Power	V_{CC}_IO		+5V
66	PHY Port B Request Data<5>	BRD5	I	TTL
67	PHY Port B Request Data<6>	BRD6	I	TTL
68	PHY Port B Request Data<7>	BRD7	I	TTL
69	PHY Port B Request Control	BRC	I	TTL
70	PHY Port B Request Parity	BRP	O	TTL
71	~Device Reset	~RST	I	TTL
72	Read/~Write	R/~W	I	TTL
73	Chip Enable	~CE	I	TTL
74	~Interrupt	~INT	O	Open Drain
75	~Acknowledge	~ACK	O	Open Drain
76	Control Bus Address<0>	CBA0	I	TTL

8.0 Connection Diagrams (Continued)

TABLE 8-1. DP83256 100-Pin PQFP Pinout Summary (Continued)

Pin No.	Signal Name	Symbol	I/O	Pin Type
77	Control Bus Address<1>	CBA1	I	TTL
78	I/O Logic Ground	GND_IO		+0V
79	I/O Logic Power	V_{CC}_IO		+5V
80	Control Bus Address<2>	CBA2	I	TTL
81	Control Bus Address<3>	CBA3	I	TTL
82	Control Bus Address<4>	CBA4	I	TTL
83	Control Bus Address<5>	CBA5	I	TTL
84	Reserved_0	RES_0		+0V
85	Reserved_1	RES_1		+5V
86	Control Bus Data<0>	CBD0	I/O	TTL
87	Core Ground	GND_CORE		+0V
88	Core Power	V_{CC}_CORE		+5V
89	Control Bus Data<1>	CBD1	I/O	TTL
90	Control Bus Data<2>	CBD2	I/O	TTL
91	Control Bus Data<3>	CBD3	I/O	TTL
92	Control Bus Data<4>	CBD4	I/O	TTL
93	Control Bus Data<5>	CBD5	I/O	TTL
94	Control Bus Data<6>	CBD6	I/O	TTL
95	Control Bus Data<7>	CBD7	I/O	TTL
96	Control Bus Data Parity	CBP	I/O	TTL
97	I/O Ground	GND_IO		+0V
98	I/O Power	V_{CC}_IO		+5V
99	Local Symbol Clock	LSC	O	TTL
100	Local Byte Clock5	LBC5	O	TTL

8.0 Connection Diagrams (Continued)

8.2 DP83257VF CONNECTION DIAGRAM

For a Pinout Summary List, refer to Table 8-1.

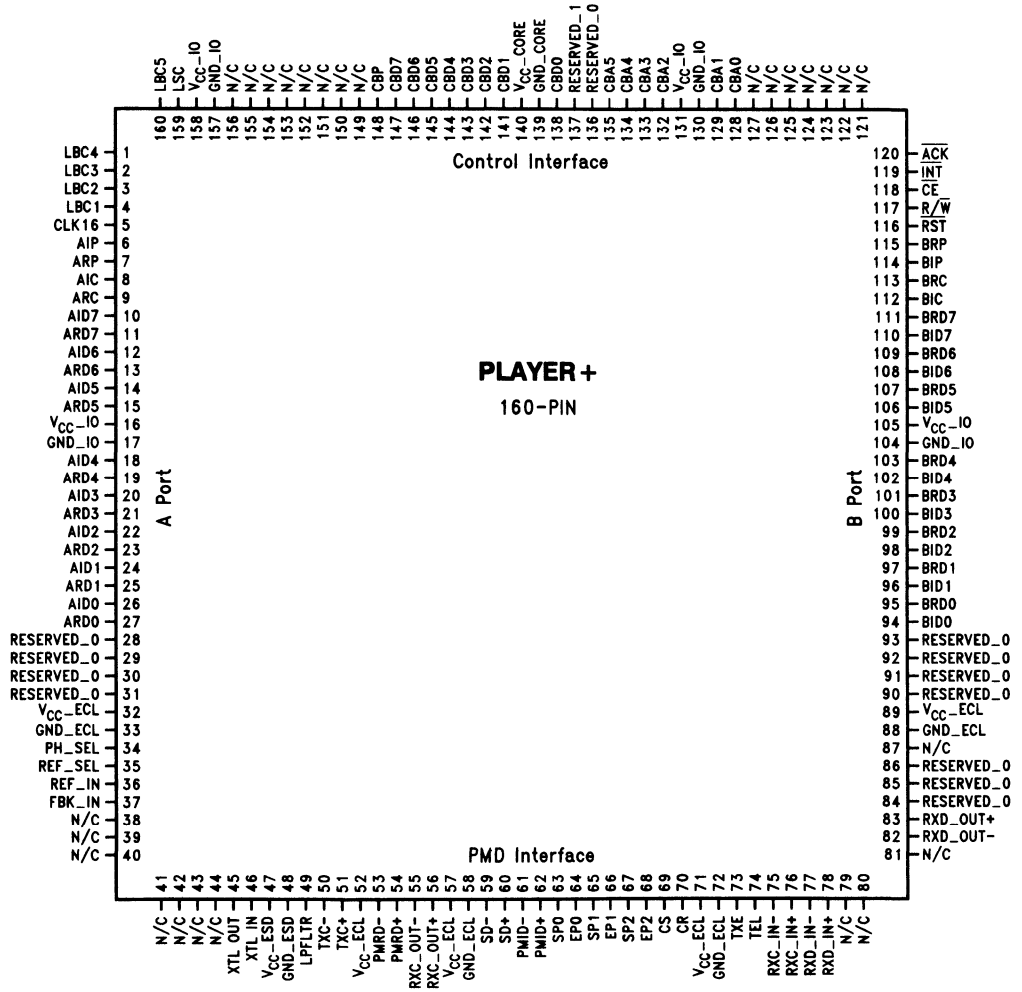

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FIGURE 8-2. DP83257VF 160-Pin JEDEC Metric PQFP Pinout

8.0 Connection Diagrams (Continued)

TABLE 8-2. DP83257 160-Pin PQFP Pinout Summary

Pin No.	Signal Name	Symbol	I/O	Pin Type
1	Local Byte Clock 4	LBC4	O	TTL
2	Local Byte Clock 3	LBC3	O	TTL
3	Local Byte Clock 2	LBC2	O	TTL
4	Local Byte Clock 1	LBC1	O	TTL
5	Clock 16/32	CLK16	O	TTL
6	PHY Port A Indicate Parity	AIP	O	TTL
7	PHY Port A Request Parity	ARP	I	TTL
8	PHY Port A Indicate Control	AIC	O	TTL
9	PHY Port A Request Control	ARC	I	TTL
10	PHY Port A Indicate Data<7>	AID7	O	TTL
11	PHY Port A Request Data<7>	ARD7	I	TTL
12	PHY Port A Indicate Data<6>	AID6	O	TTL
13	PHY Port A Request Data<6>	ARD6	I	TTL
14	PHY Port A Indicate Data<5>	AID5	O	TTL
15	PHY Port A Request Data<5>	ARD5	I	TTL
16	I/O Power	V_{CC}_IO		+5V
17	I/O Ground	GND_IO		+0V
18	PHY Port A Indicate Data<4>	AID4	O	TTL
19	PHY Port A Request Data<4>	ARD4	I	TTL
20	PHY Port A Indicate Data<3>	AID3	O	TTL
21	PHY Port A Request Data<3>	ARD3	I	TTL
22	PHY Port A Indicate Data<2>	AID2	O	TTL
23	PHY Port A Request Data<2>	ARD2	I	TTL
24	PHY Port A Indicate Data<1>	AID1	O	TTL
25	PHY Port A Request Data<1>	ARD1	I	TTL
26	PHY Port A Indicate Data<0>	AID0	O	TTL
27	PHY Port A Request Data<0>	ARD0	I	TTL
28	Reserved_0	RES_0		+0V
29	Reserved_0	RES_0		+0V
30	Reserved_0	RES_0		+0V
31	Reserved_0	RES_0		+0V
32	ECL Power	V_{CC}_ECL		+5V
33	ECL Ground	GND_ECL		+0V
34	Phase Select	PH_SEL	I	TTL
35	Reference Select	REF_SEL	I	TTL
36	Reference Input	REF_IN	I	TTL
37	Feedback Input	FBK_IN	I	TTL
38	No Connect	N/C		

8.0 Connection Diagrams (Continued)

TABLE 8-2. DP83257 160-Pin PQFP Pinout Summary (Continued)

Pin No.	Signal Name	Symbol	I/O	Pin Type
39	No Connect	N/C		
40	No Connect	N/C		
41	No Connect	N/C		
42	No Connect	N/C		
43	No Connect	N/C		
44	No Connect	N/C		
45	Crystal Output	XTAL_OUT	O	
46	Crystal Input	XTAL_IN	I	
47	ESD Power	V_{CC}_ESD		+5V
48	ESD Ground	GND_ESD		+0V
49	Loop Filter	LPFLTR	O	
50	Transmit Clock−	TXC−	O	ECL
51	Transmit Clock+	TXC+	O	ECL
52	ECL Power	V_{CC}_ECL		+5V
53	PMD Request Data−	PMRD−	O	ECL
54	PMD Request Data +	PMRD+	O	ECL
55	Receive Clock Out−	RXC_OUT−	O	ECL
56	Receive Clock Out+	RXC_OUT+	O	ECL
57	ECL Power	V_{CC}_ECL		+5V
58	ECL Ground	GND_ECL		+0V
59	Signal Detect−	SD−	I	ECL
60	Signal Detect+	SD+	I	ECL
61	PMD Indicate Data−	PMID−	I	ECL
62	PMD Indicate Data+	PMID+	I	ECL
63	Sense Pin 0	SP0	I	TTL
64	Enable Pin 0	EP0	O	TTL
65	Sense Pin 1	SP1	I	TTL
66	Enable Pin 1	EP1	O	TTL
67	Sense Pin 2	SP2	I	TTL
68	Enable Pin 2	EP2	O	TTL
69	Cascade Start	CS	I	TTL
70	Cascade Ready	CR	O	Open Drain
71	ECL Power	V_{CC}_ECL		+5V
72	ECL Ground	GND_ECL		+0V
73	PMD Transmitter Enable	TXE	O	TTL
74	PMD Transmitter Enable Level	TEL	I	TTL
75	Receive Clock In−	RXC_IN−	I	ECL
76	Receive Clock In+	RXC_IN+	I	ECL

8.0 Connection Diagrams (Continued)

TABLE 8-2. DP83257 160-Pin PQFP Pinout Summary (Continued)

Pin No.	Signal Name	Symbol	I/O	Pin Type
77	Receive Data In−	RXD_IN−	I	ECL
78	Receive Data In+	RXD_IN+	I	ECL
79	No Connect	N/C		
80	No Connect	N/C		
81	No Connect	N/C		
82	Receive Data Out−	RXD_OUT−	O	ECL
83	Receive Data Out+	RXD_OUT+	O	ECL
84	Reserved_0	RES_0		+0V
85	Reserved_0	RES_0		+0V
86	Reserved_0	RES_0		+0V
87	No Connect	N/C		
88	ECL Ground	GND_ECL		+0V
89	ECL Power	V_{CC}_ECL		+5V
90	Reserved_0	RES_0		+0V
91	Reserved_0	RES_0		+0V
92	Reserved_0	RES_0		+0V
93	Reserved_0	RES_0		+0V
94	PHY Port B Indicate Data<0>	BID0	O	TTL
95	PHY Port B Request Data<0>	BRD0	I	TTL
96	PHY Port B Indicate Data<1>	BID1	O	TTL
97	PHY Port B Request Data<1>	BRD1	I	TTL
98	PHY Port B Indicate Data<2>	BID2	O	TTL
99	PHY Port B Request Data<2>	BRD2	I	TTL
100	PHY Port B Indicate Data<3>	BID3	O	TTL
101	PHY Port B Request Data<3>	BRD3	I	TTL
102	PHY Port B Indicate Data<4>	BID4	O	TTL
103	PHY Port B Request Data<4>	BRD4	I	TTL
104	I/O Ground	GND_IO		+0V
105	I/O Power	V_{CC}_IO		+5V
106	PHY Port B Indicate Data<5>	BID5	O	TTL
107	PHY Port B Request Data<5>	BRD5	I	TTL
108	PHY Port B Indicate Data<6>	BID6	O	TTL
109	PHY Port B Request Data<6>	BRD6	I	TTL
110	PHY Port B Indicate Data<7>	BID7	O	TTL
111	PHY Port B Request Data<7>	BRD7	I	TTL
112	PHY Port B Indicate Control	BIC	O	TTL
113	PHY Port B Request Control	BRC	I	TTL
114	PHY Port B Indicate Parity	BIP	O	TTL

8.0 Connection Diagrams (Continued)

TABLE 8-2. DP83257 160-Pin PQFP Pinout Summary (Continued)

Pin No.	Signal Name	Symbol	I/O	Pin Type
115	PHY Port B Request Parity	BRP	I	TTL
116	~ Device Reset	~ RST	I	TTL
117	Read/ ~ Write	R/ ~ W	I	TTL
118	Chip Enable	~ CE	I	TTL
119	~ Interrupt	~ INT	O	Open Drain
120	~ Acknowledge	~ ACK	O	Open Drain
121	No Connect	N/C		
122	No Connect	N/C		
123	No Connect	N/C		
124	No Connect	N/C		
125	No Connect	N/C		
126	No Connect	N/C		
127	No Connect	N/C		
128	Control Bus Address<0>	CBA0	I	TTL
129	Control Bus Address<1>	CBA1	I	TTL
130	I/O Logic Ground	GND_IO		+0V
131	I/O Logic Power	V_{CC}_IO		+5V
132	Control Bus Address<2>	CBA2	I	TTL
133	Control Bus Address<3>	CBA3	I	TTL
134	Control Bus Address<4>	CBA4	I	TTL
135	Control Bus Address<5>	CBA5	I	TTL
136	Reserved_0	RES_0		+0V
137	Reserved_1	RES_1		+5V
138	Control Bus Data<0>	CBD0	I/O	TTL
139	Core Ground	GND_CORE		+0V
140	Core Power	V_{CC}_CORE		+5V
141	Control Bus Data<1>	CBD1	I/O	TTL
142	Control Bus Data<2>	CBD2	I/O	TTL
143	Control Bus Data<3>	CBD3	I/O	TTL
144	Control Bus Data<4>	CBD4	I/O	TTL
145	Control Bus Data<5>	CBD5	I/O	TTL
146	Control Bus Data<6>	CBD6	I/O	TTL
147	Control Bus Data<7>	CBD7	I/O	TTL
148	Control Bus Data Parity	CBP	I/O	TTL
149	No Connect	N/C		
150	No Connect	N/C		
151	No Connect	N/C		

TABLE 8-2. DP83257 160-Pin PQFP Pinout Summary (Continued)

Pin No.	Signal Name	Symbol	I/O	Pin Type
152	No Connect	N/C		
153	No Connect	N/C		
154	No Connect	N/C		
155	No Connect	N/C		
156	No Connect	N/C		
157	I/O Ground	GND_IO		+0V
158	I/O Power	V_{CC}_IO		+5V
159	Local Symbol Clock	LSC	O	TTL
160	Local Byte Clock5	LBC5	O	TTL

9.0 Package Information

The information contained in this section describes the two packages used for the PLAYER+ device.

Land pattern information is provided to assist in surface mount layout using each of the available PLAYER+ device packages.

Mechanical drawings of each of the packages are also provided.

9.1 LAND PATTERNS

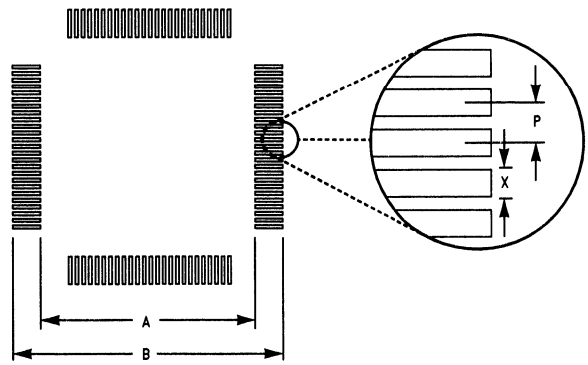

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FIGURE 8-1. Layout Land Patterns

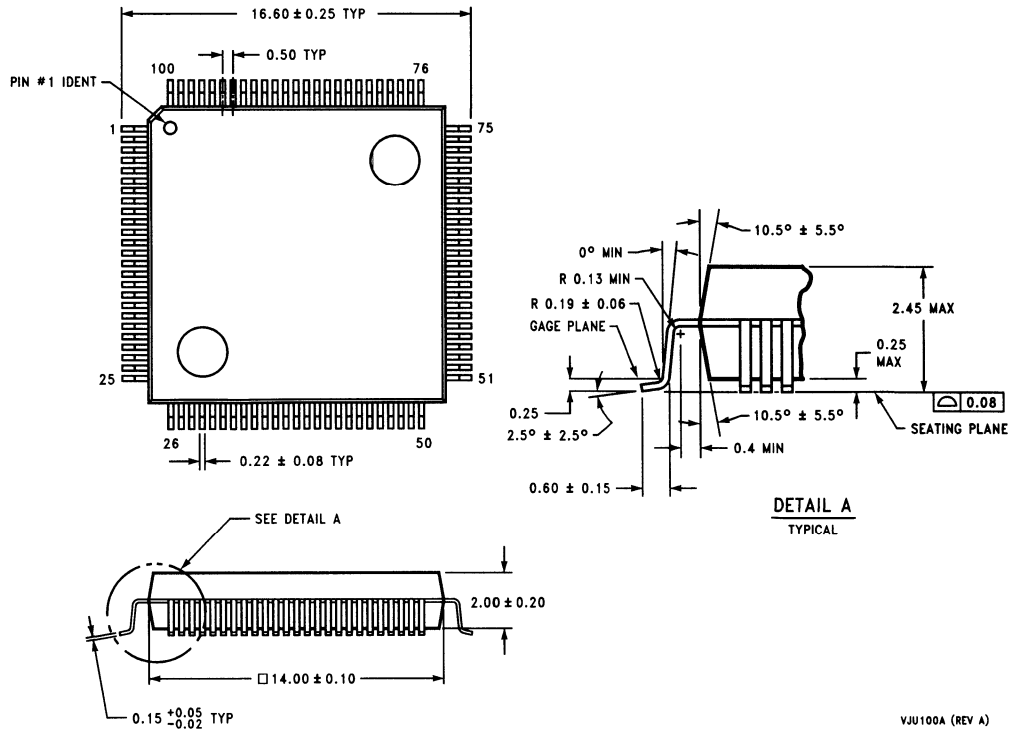
TABLE 8-1. Layout Land Pattern Dimensions

Device	A (mm)	B (mm)	P (mm)	X (mm)
DP83256VF 14mm x 14mm x 2.0mm 100-lead JEDEC FPQFP	14.60	18.45	0.50	0.35
DP83257VF 28mm x 28mm x 3.42mm 160-lead JEDEC MQFP	28.90	33.40	0.65	0.45

9.2 MECHANICAL DRAWINGS

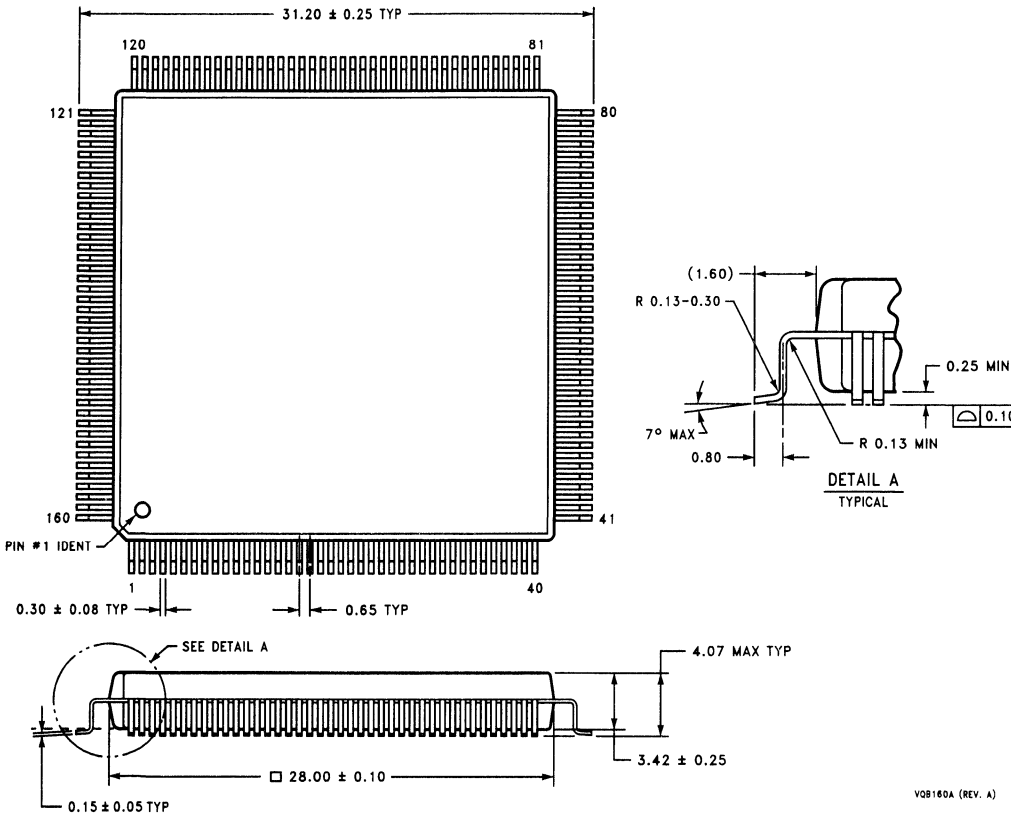
The following two pages contain the mechanical drawings for each of the available PLAYER+ device packages.

Physical Dimensions inches (millimeters)



Plastic Quad Flatpak (VJU)
Order Number DP83256VF
NS Package Number VJU100A

Physical Dimensions inches (millimeters) (Continued)



Plastic Quad Flatpak (V)
Order Number DP83257VF
NS Package Number VQB160A

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DP83220 CDL
Twisted Pair FDDI
Transceiver Device

National Semiconductor

ADVANCE INFORMATION
October 1992

DP83220
CDL™ Twisted Pair FDDI Transceiver Device

General Description

The Copper Data Link (CDL) Transceiver is an integrated circuit designed to interface directly with the National Semiconductor FDDI Chip Set or other FDDI PHY silicon, allowing low cost FDDI compatible data links over copper based media. The DP83220 Transceiver, with the proper compensation selected, will allow links of up to 100 meters over both Shielded Twisted Pair (STP) and Datagrade unshielded Twisted Pair (DTP). CDL surpasses a Bit Error Rate (BER) of $<1 \times 10^{-12}$ over both STP and DTP. The CDL is designed to meet the SDDI specification for FDDI transmission across Type 1 STP cable when used in conjunction with the appropriate transformer/filter module from Pulse Engineering.

Features

- Fully compatible with current FDDI PHY standard
- Fully compatible with the SDDI PMD specification
- Requires a single +5V supply
- Isolated TX and RX power supplies for minimum noise coupling
- Allows use of Type 1 STP and Category 5 DTP cables
- No Transmit Clock required
- Loopback feature for board diagnostics
- Link Detect input provided

Block Diagram

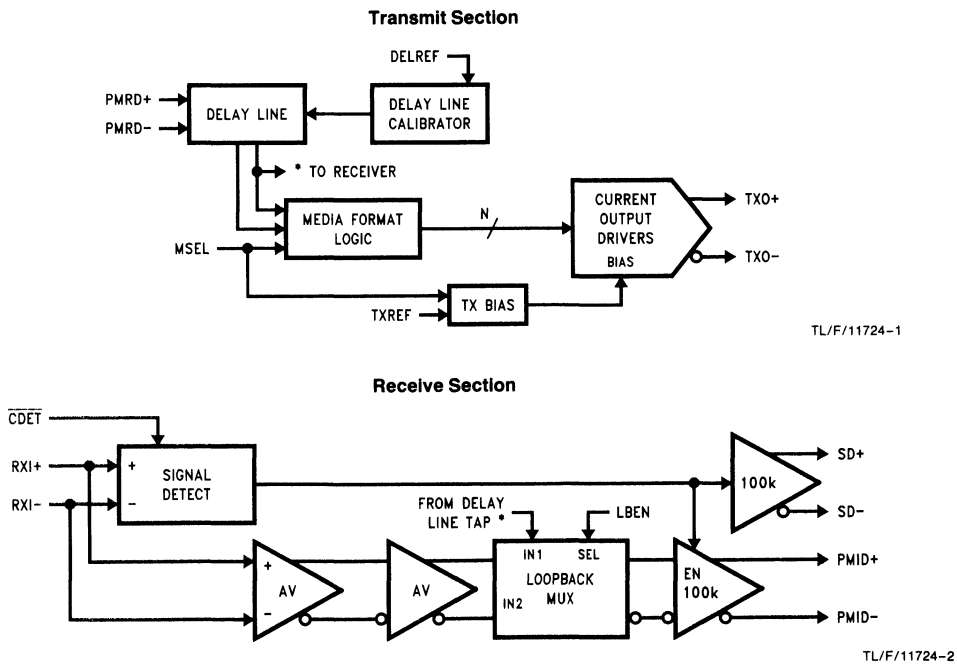


FIGURE 1. DP83220 Transceiver Block Diagram

RRD-B20M102/Printed in U. S. A.

1.0 Functional Description

The CDL Transceiver consists of nine major functional blocks as shown in *Figure 1.* The Transmit section includes the following: the Delay Line, the Delay Line Calibrator, the Media Format Logic, and the Current Output Driver circuitry with its bias circuitry. The Delay Line accepts the NRZI encoded data from the PMRD± pins and provides a short "memory" of the bit that preceded the bit currently being transmitted. The Delay Line Calibrator allows the use of an external resistor which governs the time calibration of the delay line. The Delay Line outputs the data via taps which are tied to the Media Format Logic. The encoding logic is dependent on the state of the Media Select pin. The encoded data is routed to the Current Output Driver, through the TXO± output pins and transformer coupled to the media.

The Receive section consists of the following: a differential input amplifier, Signal Detect circuitry, a Loopback Multiplexer, and differential 100K output drivers for data and Signal Detect. The Receive signal is input to the RXI± pins from the receive isolation transformer. The input signal is sensed by the Signal Detect circuit. The input signal also drives a differential input amplifier whose output is coupled to the Loopback Mux logic. The 'sel' input which is driven by LBEN controls which data stream, RXI± or Loopback data, is routed to the differential 100K Output Driver. When in Loopback mode, the Signal Detect output driver is forced true. When receiving data from copper media, the signal detect circuit provides valid states to the Signal Detect output driver depending on the amplitude of the incoming signal and also allows the PMID± outputs to switch. Cable Detect is the final gating function for data reception. If no media is detected, the transceiver will generate a logic low Signal Detect which will inhibit data reception by the PHY.

1.1 SDDI OPERATION

The CDL allows full compatibility with the current SDDI specification. By allowing the MSEL pin to float, which forces the pin to $V_{CC}/2$ internally, the SDDI mode of operation is selected. The appropriate transmit voltage amplitude must also be set by selecting a value of 2.6 kΩ for the TXREF resistor.

Finally, it is important to note that the CDL must be used in conjunction with the Pulse Engineering 8.3 magnetics module in order to conform to the current SDDI specification. No special terminations are required in connecting the Pulse Engineering 8.3 module to the CDL. (Refer to the typical SDDI schematic, *Figure 9.*)

2.0 Pinout Summary

Signal	Pin No.	Description	Type
V_{CC}	13, 26	V_{CC}	Supply
GND	14, 22	GND	Supply
RXV_{CC}	4, 27	Receive V_{CC}	Supply
RXGND	3, 28	Receive GND	Supply
TXV_{CC}	5, 11	Transmit V_{CC}	Supply
TXGND	7, 10	Transmit GND	Supply
$EXTV_{CC}$	23	External V_{CC}	Supply
RXI±	2, 1	Receive Data Inputs	Current In
PMID±	25, 24	Physical Media Indicate Data	ECL Out
PMRD±	15, 16	Physical Media Request Data	ECL In
TXO±	9, 8	Transmit Data Outputs	Current Out
SD±	20, 21	Signal Detect Outputs	ECL Out
TXREF	6	Transmit Amplitude Reference	Current Out
DELREF	12	Delay Line Calibration Reference	Current Out
LBEN	19	Loopback Enable	CMOS In
MSEL	17	Media Select	3-Level Select
$\overline{CDET}$	18	Cable Detect Bar	CMOS Schmitt Trigger In

3.0 Pin Definitions

V_{CC} (13,26): Positive power supply for the 100K ECL compatible circuitry. The Transceiver operates from a single +5 V_{DC} power supply.

GND (14,22): Return path for the 100K ECL compatible circuitry power supply.

RXV_{CC} (4,27): Positive power supply for the small signal receive circuitry. This power supply is intentionally separated from others to eliminate receive errors due to coupled supply noise.

RXGND (3,28): Return path for the receive power supply circuitry. This Power supply return is intentionally separated from others to eliminate receive errors due to coupled supply noise.

TXV_{CC} (5,11): Positive power supply required by the analog portion of the transmit circuitry. This power supply is intentionally separated from the others to prevent supply noise from coupling to the transmit outputs.

TXGND (7,10): Return path for the analog transmit power supply circuitry. This supply return is intentionally separated from others to prevent supply noise from being coupled to the transmit outputs.

$EXTV_{CC}$ (23): Positive power supply for receiver output circuitry.

RXI± (2,1): Balanced differential line receiver inputs. Signals meeting the input threshold for a given media type are output through PMID± as differential ECL.

PMID± (25,24): 100K ECL compatible differential outputs used as the source of the receive data for the DP83231 Clock Recover Device (CRD™).

PMRD± (15,16): Differential 100K compatible 4B5B NRZI transmit data inputs originating from the DP83251/55 Physical Layer Device (PLAYER™).

TXO± (9,8): Differential current driver outputs precompensated for twisted pair cable.

SD± (20,21): Differential 100K ECL compatible Signal Detect outputs indicating that a valid signal is present at the RXI± inputs.

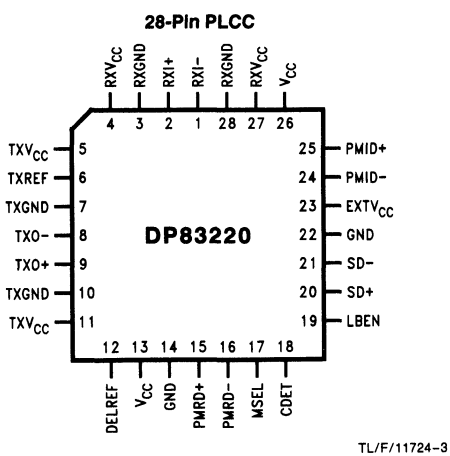
DELREF (12): A resistor is connected between this pin and GND. The value of this resistor controls the current into the delay line calibrator which, in turn controls the delay time of the delay line.

TXREF (6): A resistor is connected between this pin and TXGND. The value of this resistor controls the signal amplitude of the TXO± data which drives the twisted pair.

LBEN (19): TTL compatible CMOS Loopback Enable input pin selects the internal loopback path which effectively routes the PMRD± data to the PMID± differential outputs.

MSEL (17): The Media Select input controls the compensation and output current required to drive to 100 meters of either STP or DTP media. This is a tri-level control pin. When forced to a low voltage, STP compensation is selected. Forcing a high voltage level will select the DTP compensation mode. Forcing a median voltage allows the device to operate in the transparent mode by deasserting pre-emphasis.

$\overline{CDET}$ (18): The Cable Detect input is provided to support the option of external Cable Detection circuitry. With $\overline{CDET}$ low, the CDL transceiver functions normally. When $\overline{CDET}$ is high, the signal detect output is forced low which inhibits data reception by the PHY. The exception is in the case of Loop Back, where Signal Detect is forced high regardless.



Order Number DP83220V
See NS Package Number V28A

FIGURE 2. Pin Configuration

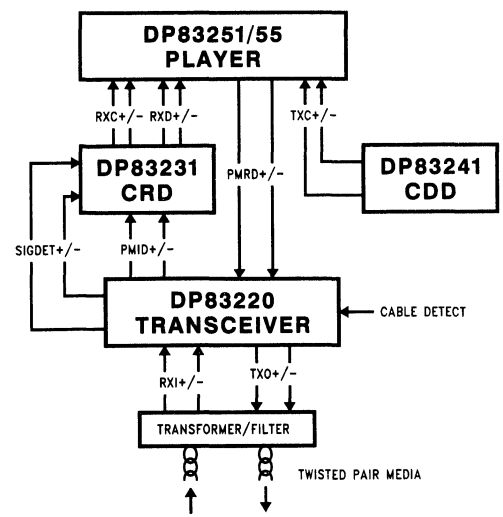


FIGURE 3. System Connection Diagram

4.0 Electrical Characteristics

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC}	Logic Power	Referenced to GND	−0.5		6.0	V
RXV_{CC}	Received Power	Referenced to RXGND	−0.5		6.0	V
TXV_{CC}	Transmit Power	Referenced to TXGND	−0.5		6.0	V
$EXTV_{CC}$	ECL Output Power	Referenced to GND	−0.5		6.0	V
I_{ECL}	DC Output Current (High)				−50	mA
ESD				TBD		
$T_{storage}$	Storage Temperature		−65		+150	°C

4.1 RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC}	Supply Voltage		4.5	5.0	5.5	V
T_A	Operating Temperature		0	25	70	°C
P_D	Power Dissipation			600		mW

4.2 DC ELECTRICAL CHARACTERISTICS T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IHt}	TTL High Level Input		2.0			V
V_{ILt}	TTL Low Level Input				0.8	V
$V_{IHschmitt}$	Schmitt High Level Input		3.7			V
$V_{ILschmitt}$	Schmitt Low Level Input				1.5	V
V_{IHmsel}	MSEL High Level Input		3.7			V
V_{ILmsel}	MSEL Low Level Input				1.5	V
V_{IMmsel}	MSEL Middle Level Input			$V_{CC}/2$		V
V_{IHe}	ECL High Level Input		V_{CC} − 1165		V_{CC} − 870	mV
V_{ILe}	ECL Low Level Input		V_{CC} − 1830		V_{CC} − 1475	mV
V_{OHe}	ECL High Level Output	Refer to *Figure 4*	V_{CC} − 1035		V_{CC} − 870	mV
V_{OLe}	ECL Low Level Output	Refer to *Figure 4*	V_{CC} − 1830		V_{CC} − 1605	mV
I_{CC1}		Refer to *Figure 4*		90		mA
I_{CCT}	Total Supply Current	Refer to *Figure 4*		145		mA
I_{TXO1}	Transmit Current 1	Transmit Current / 100Ω Z_O			20	mA
I_{TXO2}	Transmit Current 2	Transmit Current / 150Ω Z_O			15	mA
SD_{THon}	Sig Det Turn-On Threshold	Refer to *Figure 5*, Note 1	60			mV
SD_{THoff}	Sig Det Turn-Off Threshold	Refer to *Figure 5*, Note 1			15	mV

4.3 AC ELECTRICAL CHARACTERISTICS T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{TXr/f}$	TX Driver Rise and Fall	Into 25Ω in Parallel with 50 pF		1.6		ns
$t_{TXr/f}$	TX Driver Rise and Fall	Into 37.5Ω in Parallel with 50 pF		2.5		ns
t_{TXpd}	TX Propagation Delay	From PMRD± to TXO±		6		ns
t_{RXpd}	RX Propagation Delay	From RXI± to PMID±		10		ns
T_{TXskew}	TX Driver Skew			0		ps

Note 1: Subject to change.

4.0 Electrical Characteristics (Continued)

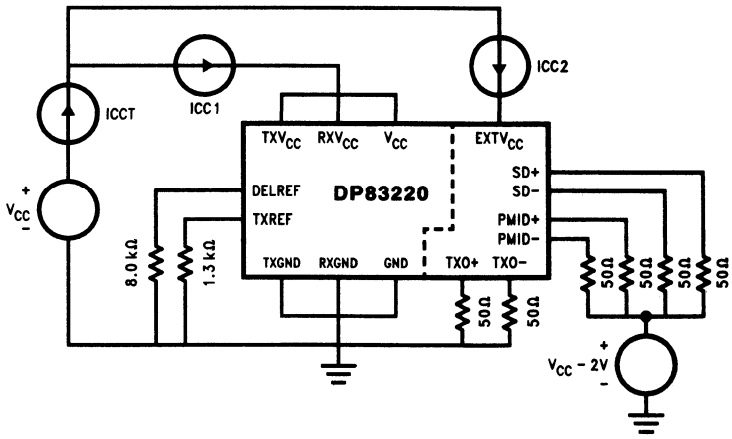


FIGURE 4. I_{CC} Diagram

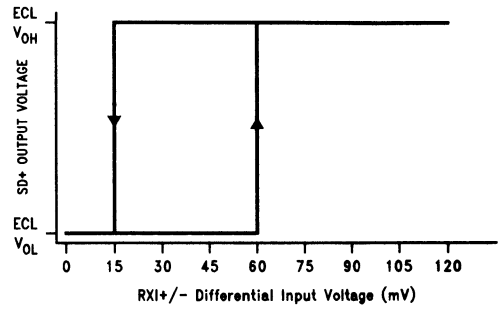


FIGURE 5. Signal Detect Threshold

4.0 Electrical Characteristics (Continued)

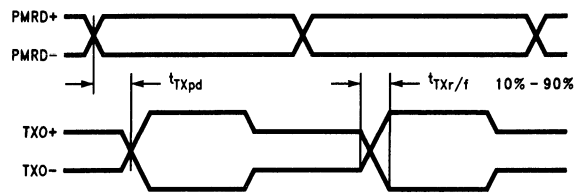


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FIGURE 6. Transmit Timing

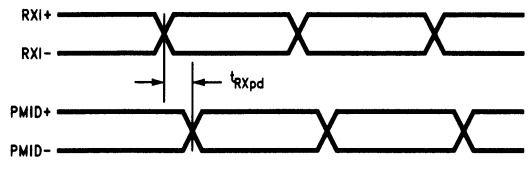

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FIGURE 7. Receive Timing

4.0 Electrical Characteristics (Continued)

4.3 TRANSMIT DATA AND CURRENT DRIVER OUTPUT

TXDn	TXDn−1	I_{TXO+}	I_{TXO-}
0	0	$(I_1)\ I_{max}$	$(I_2)\ I_{max}$
0	1	$(I_1 + I_2)\ I_{max}$	0
1	0	0	$(I_1 + I_2)\ I_{max}$
1	1	$(I_2)\ I_{max}$	$(I_1)\ I_{max}$

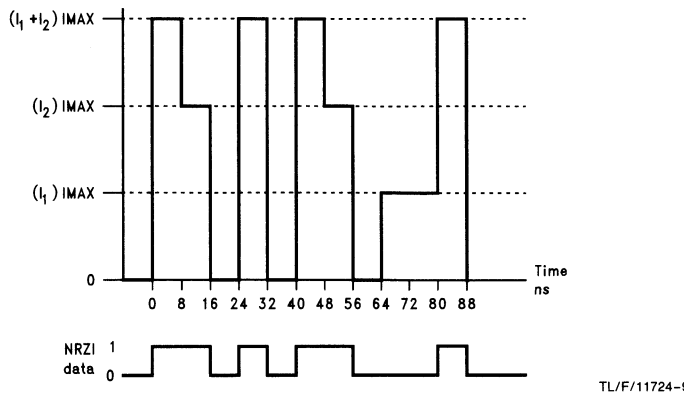

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FIGURE 8. Typical Pre-Emphasized Current Waveform, I_{TXO+}

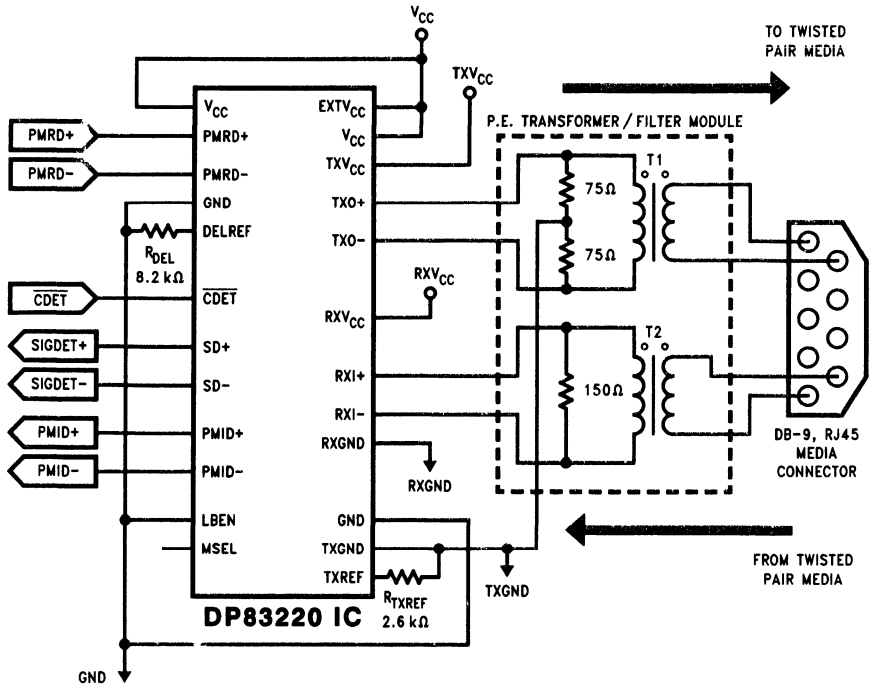
TABLE I. Media Select

Mode	MSEL
STP	<1.5V
DTP	>3.7V
SDDI	Float

TABLE II. Data Paths and Signal Detect

LBEN	$\overline{CDET}$	Data @ PMID±	SD+
0	1	RXI±	0
0	0	RXI±	1
1	1	PMRD±	1
1	0	PMRD±	1

Note: This table assumes that minimum signal's levels required by Signal Detect have been met.



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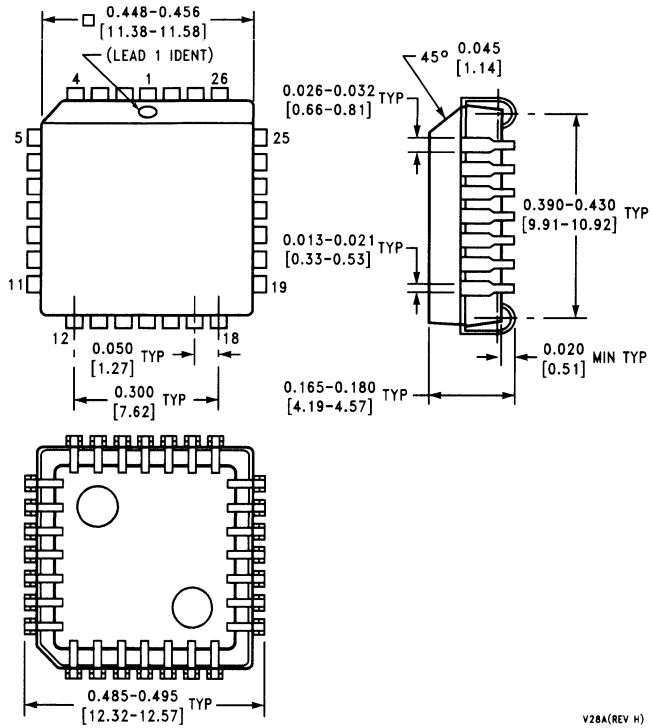
Refer to the Pulse Engineering datasheet for detailed information on the 8.3 SDDI magnetics module.

FIGURE 9. Typical Schematic for SDDI Application

Physical Dimensions inches (millimeters)



28-Pin Plastic Leaded Chip Carrier (V)
Order Number DP83220V
NS Package Number V28A

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